



AiP1723

20 SEG/4 COM LCD Display Driver with Keyboard Scan Ports and PWM

Product Specification

Specification Revision History:

Version	Data	Description
2015-05-A1	2015-05	New
2024-08-B1	2024-08	Update the template; Modify the content



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1、General Description

AiP1723 is a driver with key scan interface control dedicated circuit, integrated MCU digital interface, data latches, LCD driver, keyboard scanning, Symphony backlight driver circuit. It is mainly used in segment code LCD display applications that require extended keys and backlight electronic coded switch functions, such as home video systems, wall-hung boilers and other products of the display driver.

Features:

- Using low-power CMOS process
- Display mode: 4 × 20 LCD driver
- Key Scan: Up to 4 × 3
- 4 LED Driver with 64 PWM, can be used in LCD backlight driver Symphony
- 2 universal input interface can be connected wave wheel electronic code switch
- 1/2 or 1/3 LCD drive bias Optional
- LCD operating voltage is adjustable for adjusting the brightness of the LCD screen
- Serial interface: CLK, STB, DIO
- Oscillation mode: Built-in RC oscillator (typical oscillation frequency 128KHz ± 5%)
- Built-in power-on reset circuit
- Package: SOP32

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP1723SA32.TB	SOP32	AiP1723	20 PCS/tube	80 tube/box	1600 PCS/box	Dimensions of plastic enclosure: 21.0mm×7.5mm Pin spacing: 1.27mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP1723SA32.TR	SOP32	AiP1723	1250 PCS/reel	1250 PCS/box	Dimensions of plastic enclosure: 21.0mm×7.5mm Pin spacing:1.27mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

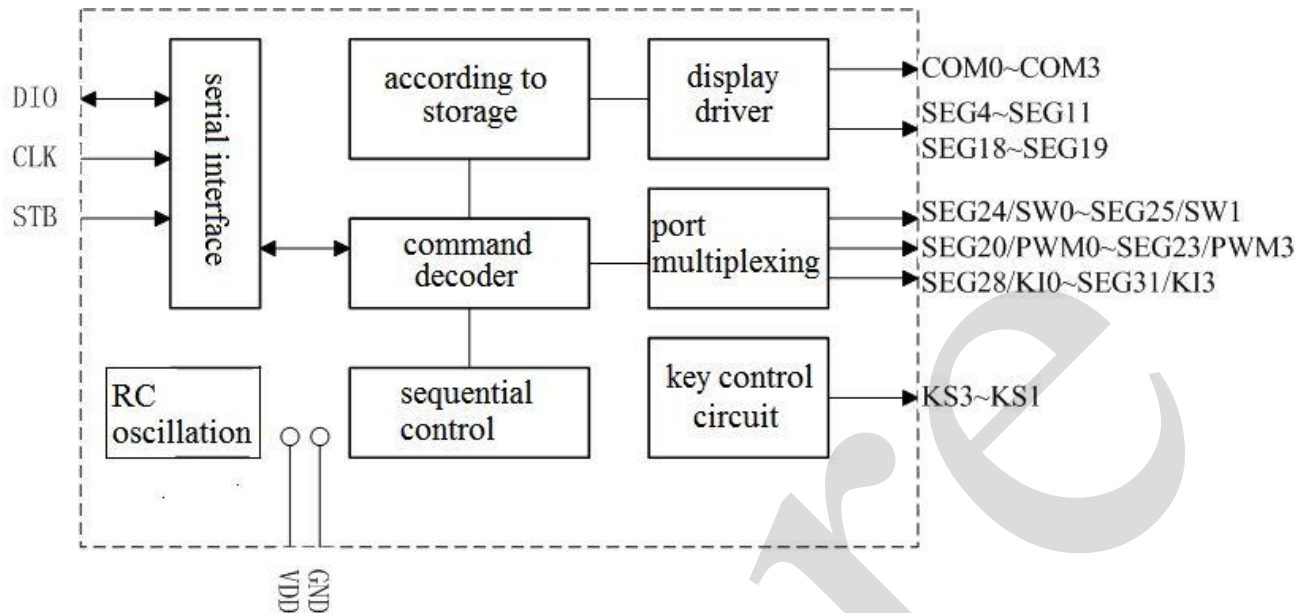


Figure 1

2.2、Pin Configurations

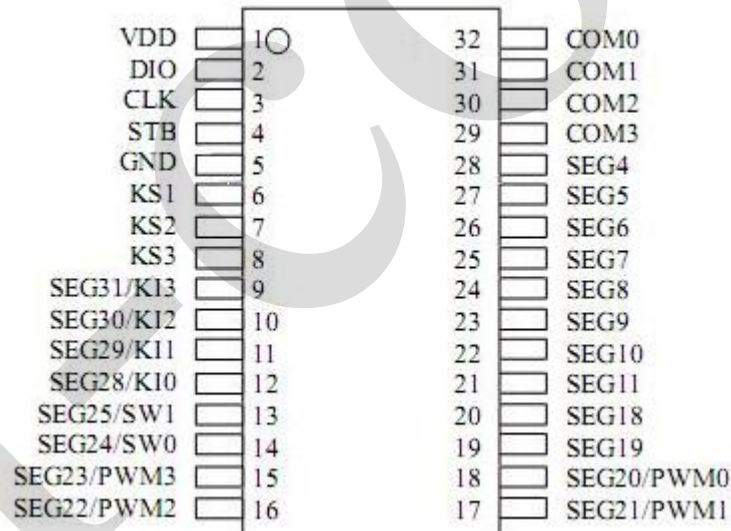


Figure 2

**2.3、Pin Description**

Pin No.	Pin Name	Description
1	VDD	Power supply
2	DIO	Serial data line This pin inputs serial data at the rising edge of the shift clock(starting from the lower)
3	CLK	Clock input pin. This pin reads serial data at the rising edge and outputs data at the falling edge.
4	STB	Serial interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH",CLK is ignored.
5	GND	Ground Pin
6~8	KS1~KS3	Key data input Pins The data sent to these pins are latched at the end of the display cycle.(Internal Pull-Low Resistor)
7~12	SEG31/KI3 ~ SEG28/KI0	Segment Output Pins(P-channel, open drain) Also acts as the Key Source
13~14	SEG25/SW1 ~ SEG24/SW0	Segment output / Universal input composite port
15~18	SEG23/PWM3 ~ SEG20/PWM0	Segment output / PWM output Composite port
19~28	SEG19~SEG18,SEG11~SEG4	Segment output LCD segment drive output
29~32	COM3 ~ COM0	Public-ended output LCD Public-ended drive output

Note:

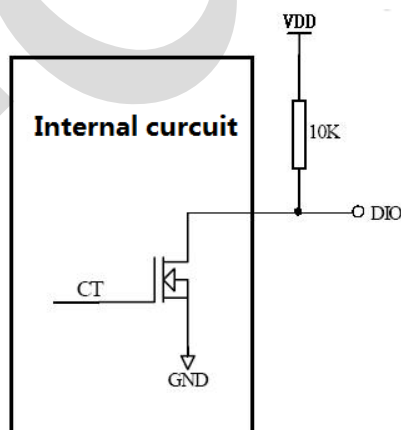


Figure 3

**3、Electrical Parameter****3.1、Absolute Maximum Ratings**(T_{amb}=25℃, all voltage referenced to GND, unless otherwise specified.)

Parameter	Symbol	Conditions	Value	Unit
Logic Supply Voltage	VDD	-	-0.5 to +6.0	V
Logic input voltage	VIN	-	-0.5 to VDD + 0.5	V
Ambient temperature	T _{amb}	-	-40 to +85	℃
Storage temperature	T _{stg}	-	-65 to +150	℃
Soldering Temperature	T _L	10s	250	℃

3.2、Recommended Operating Range(T_{amb}=-40℃ to +85℃, GND=0V.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	VDD	2.7	5	5.5	V
High-level input voltage	V _{IH}	0.7VDD	-	VDD	V
Low-level input voltage	V _{IL}	0	-	0.2VDD	V

3.3、Electrical Characteristics**3.3.1、DC Characteristics**(T_{amb}=-40℃ to +85℃, GND=0V, VDD=5V.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low-level output current	I _{OL1}	COM0~COM3, VO=0.5V	150	250	-	uA
High-level output current	I _{OH1}	COM0~COM3, VO=4.5V	-120	-150	-	uA
Low-level output current	I _{OL2}	COM0~ COM3, VO=0.5V	120	200	-	uA
High-level output current	I _{OH2}	COM0~ COM3, VO=4.5V	-70	-100	-	uA
Low-level output current	I _{OL3}	PWM0~PWM3 (output state), VO = 1V	30	60	-	mA
PWM High-level output current	I _{OH3}	PWM0~PWM3 (set to output mode), VO=3V	-15	-25	-	mA
KS Low-level output current	I _{OL4}	KS1~KS3 (set to output mode), VO=0.5V	15	30	-	mA
KS High-level output current	I _{OH4}	KS1~KS3 (set to output mode), VO=3V	-15	-25	-	mA
DIO Low-level output current	I _{DO}	VO=0.4V, DOUT	4	-	-	mA
KI/SW Pull-down resistor	R _L	KI0~KI3/SW0~SW1 (set to input mode)	20	-	80	KΩ
Input current	I _{IN}	VIN=VDD/GND CLK, DIO, STB	-	-	±1	uA
High-level output current	V _{IH}	CLK, DIO, STB	0.7VDD	-	-	V
Low-level output current	V _{IL}	CLK, DIO, STB	-	-	0.2VDD	V
Hysteresis voltage	V _H	CLK, DIO, STB	-	0.35	-	V
Dynamic current consumption	I _{DDdyn}	No load, display off	-	-	1	mA



3.3.2、Switching Characteristics

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, GND=0V, VDD=5V.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC}	-	-	128	-	KHz
Propagation delay	t_{PLZ}	CLK $\rightarrow$ DIO $C_L=15\text{pF}$, $R_L=10\text{K}\Omega$	-	-	300	ns
	t_{PZL}	-	-	-	100	ns
Maximum clock frequency	f_{max}	Duty=50%	1	-	-	MHz
Input capacitance	C_I	CLK, DIO, STB	-	-	15	pF

3.3.3、Timing Characteristics

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, GND=0V, VDD=5V.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	PW_{CLK}	-	400	-	-	ns
STB pulse width	PW_{STB}	-	1	-	-	us
Set-up time for data	t_{SETUP}	-	100	-	-	ns
Hold time for data	t_{HOLD}		100	-	-	ns
Propagation delay CLK to STB	$t_{CLK-STB}$	CLK $\uparrow \rightarrow$ STB $\uparrow$	1	-	-	us
Wait time	T_{wait}	CLK $\uparrow \rightarrow$ CLK $\downarrow$	1	-	-	us

4、Function Description

4.1、Switching Characteristic Waveform

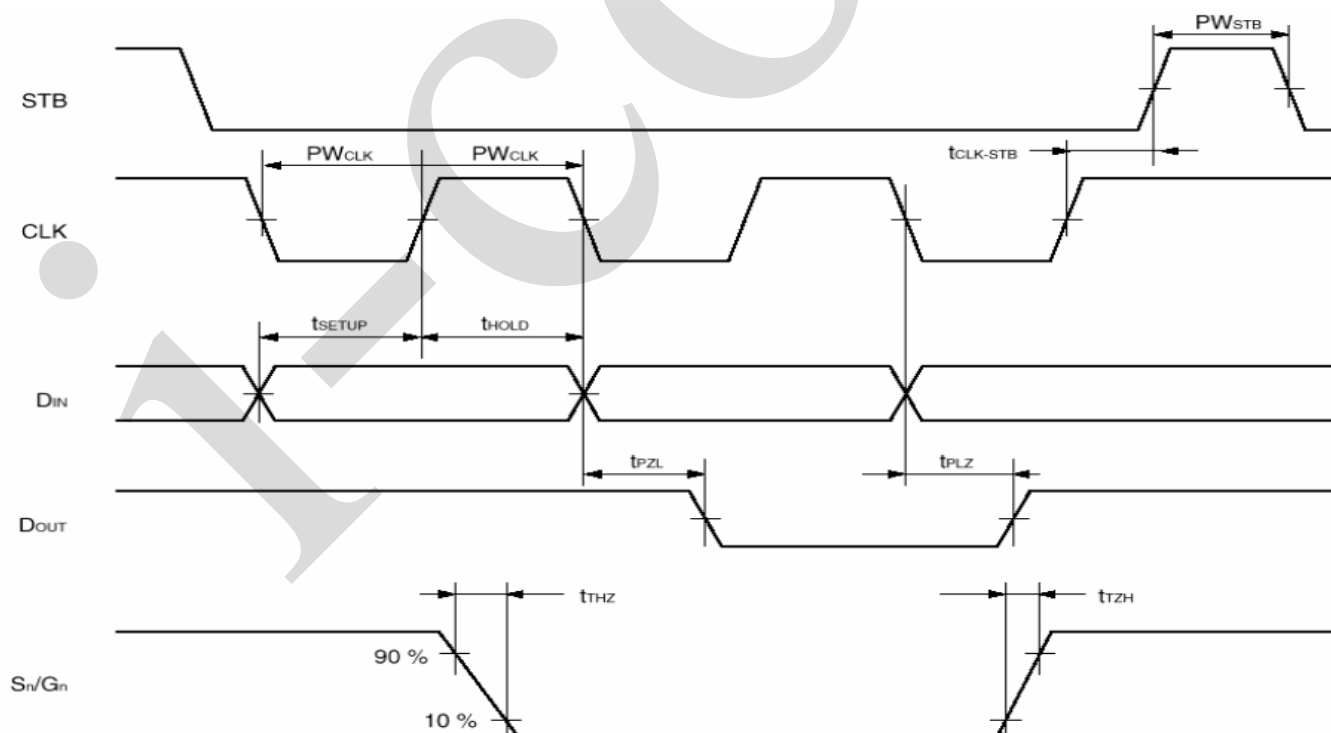


Figure 4



4.2、Display Mode And RAM Address

Data transmitted from an external device to AiP1723 via the serial interface are stored in the Display RAM and are assigned addresses.

COM0	COM1	COM2	COM3	COM0	COM1	COM2	COM3	RAM Address
SEG4				SEG5				02H
SEG6				SEG7				03H
SEG8				SEG9				04H
SEG10				SEG11				05H
SEG18				SEG19				09H
SEG20				SEG21				0AH
SEG22				SEG23				0BH
SEG24				SEG25				0CH
SEG26				SEG27				0DH
SEG28				SEG29				0EH
SEG30				SEG31				0FH
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	

4.3、Key Matrix & Key Input DATA Storage RAM

Key matrix consists of 3*4 array as shown below:

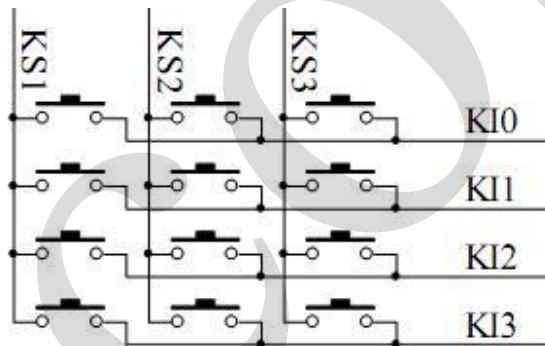


Figure 5

Each data entered by each key is stored as follows and read by a READ command, starting from the last significant bit.

KI0/ SEG28	KI1/ SEG29	KI2/ SEG30	KI3/ SEG31	KI0/ SEG28	KI1/ SEG29	KI2/ SEG30	KI3/ SEG31	
X				KS1				00H
KS2				KS3				01H
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	



4.4、Port Control Register

4.4.1、PWM Register Instructions

Command (B1B0)	Register	High	Low
00	PWM0	XXb5b4_b3b2b1b0	
01	PWM1	XXb5b4_b3b2b1b0	
10	PWM2	XXb5b4_b3b2b1b0	
11	PWM3	XXb5b4_b3b2b1b0	

PWM0-PWM3 register instructions:

b5b4_b3b2b1b0	PWM Pulse Width Setting
00H	0
01H ~ 3EH	1/64 ~ 62/64
3FH	1

Note: When power is turned on, the initial state of all registers is set at 0.

4.4.2、SW Input Register Instruction

Read by a READ command, starting from the last significant bit.

b0	b1	b2	b3	b4	b5	b6	b7
SW0	SW1	-	-	0	0	0	0

4.5、Commands Description

A command is first byte(b0 to b7)inputted to AiP1723 via the DIO Pin after STB Pin has changed from high to low state.

B7	B6	Instructions
0	0	Display setting command
0	1	Data setting commands
1	0	Display control commands
1	1	Address setting commands

4.5.1、Display Setting Commands

MSB				LSB			
0	0	b5	b4	b3	b2	b1	b0

b1b0	General input port/SEG output settings
00	SEG24, SEG25
01	SEG24, SEG25
10	SEG24, SEG25
11	SW0, SW1



b5b4	PWM output port/SEG output setting
00	SEG20, SEG21, SEG22, SEG23
01	SEG20, SEG21, SEG22, PWM3
10	SEG22, SEG23, PWM2, PWM3
11	PWM0, PWM1, PWM2, PWM3

b3b2	Key input port/ SEG output setting
00	SEG28, SEG29, SEG30, SEG31
01	SEG28, SEG29, SEG30, KI3
10	SEG28, SEG29, KI2, KI3
11	KI0, KI1, KI2, KI3

Note: When power is turned on, the initial state of all registers is set at 0.

4.5.2、Data Setting Commands

MSB				LSB				Function	Instructions
B7	B6	B5	B4	B3	B2	B1	B0		
0	1	Not relevant, write 0		-	-	0	0	Data write & read mode setting	Writing data to the display register
0	1			-	-	0	1		Writing data to PWM register
0	1			-	-	1	0		Reading scanning data
0	1			-	-	1	1		Read key data
0	1			-	0	-	-	Address increment mode setting	Increment address after data has been written
0	1			-	1	-	-		Fixed address
0	1			0	-	-	-	Testing mode settings	Normal operation mode
0	1			1	-	-	-		Test mode

4.5.3、Address Setting

MSB				LSB				Address
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	Not relevant, write 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH
1	1			1	1	1	0	0EH
1	1			1	1	1	1	0FH

Note: Address setting commands are used to set the address of the display memory. The address is considered



valid if it has a value of 00H to 0FH.

4.5.4、Display Control

MSB				LSB			
1	0	b5	b4	b3	b2	b1	b0

b5: System clock selection; when set to 0, the clock frequency is 256KHz and the display frame rate is 60Hz; When set to 1, the clock frequency is 830kHz and the display frame rate is 200Hz.

b4: Display switch position; 1: Display on 0: Display off

b3: LCD drive bias setting bits; 1: 1/2 bias 0: 1/3 bias

b2b1b0: LCD Operating voltage setting bit:

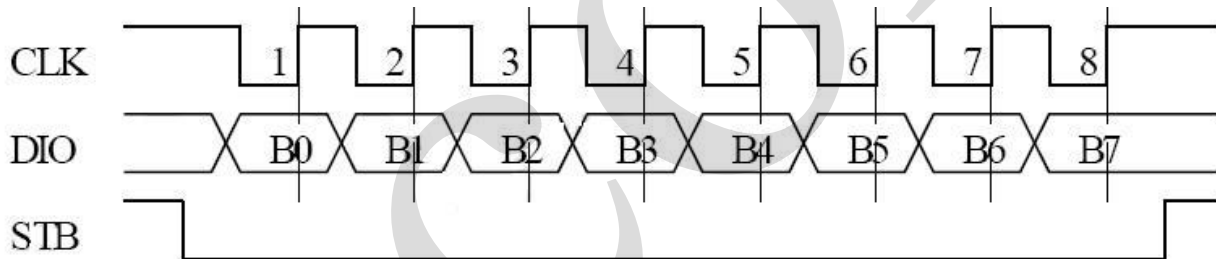
When b2b1b0 equal to 111, the working voltage equal to VDD (VDD for the chip's operating voltage).When VDD is equal to 5V and b3 is equal to 1, regulating voltage is of range of about 2.24V-5V; b3 is equal to 0 (1/3 bias), regulating voltage range is about 2.88-5V.

Note: After power on, b5b4b3b2b1b0 is set to 000111.

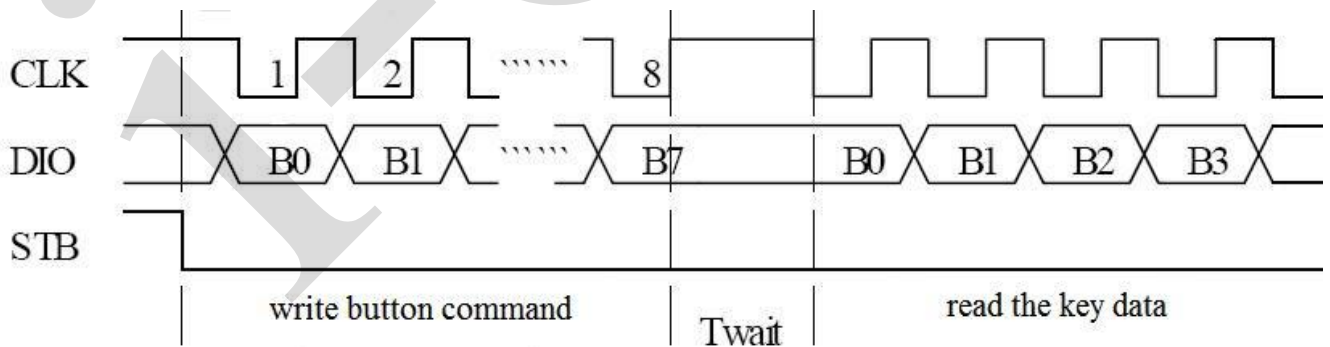
4.6、Serial Data Transmission Format

Read and receive a BIT are the operation of rising clock edge.

4.6.1、Data Reception (write data)



4.6.2、Data Read (read data)



Note: When reading data, it requires a wait time T_{wait} (minimum 1us) from the serial clock CLK first eight rising edge to CLK falling.



4.7、Key Sweep, PWM, SW Applications

4.7.1、Key Sweep

Key scan is carried out automatically by AiP1723, without user control, the user need only read in accordance with the timing key. It needs two display period to complete a key sweep , a display period takes about $8 \times 500\mu s$ and pressed two different keys in 8MS, both key value are showed when the button keys is pressed firstly.

As shown in Figure 6 was observed with an oscilloscope output key KS1 and KS2 sweep waveform, showed in Figure 7.

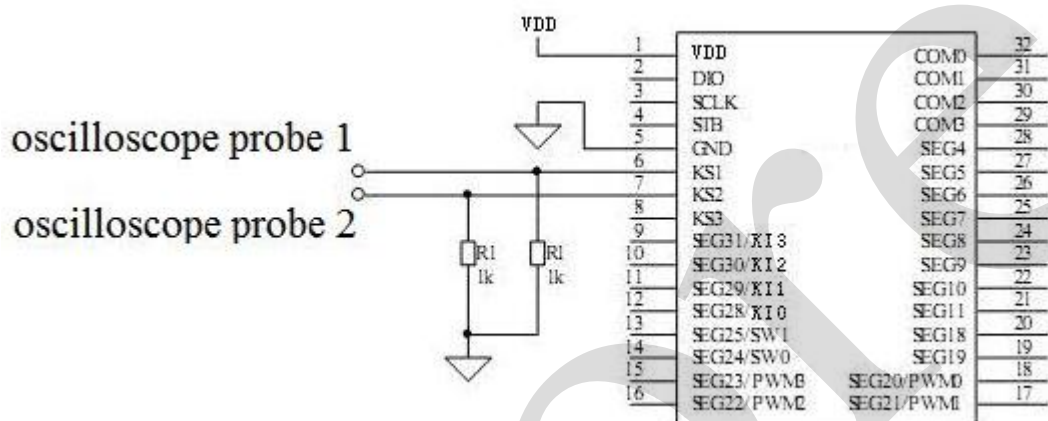


Figure 6

When the circuit scan at the keyboard scan the KSN waveform is below:



Figure 7

Note: T_{disp} is related to the oscillation frequency of the circuit, AiP1723 has passed several perfect by us, and the oscillation frequency is not exactly the same. $500\mu s$ is only a reference, the value is subject to the actual measurement.



4.7.2、PWM Output

The control the PWM output is accordance with the flow of Figure 8. It can be observed with an oscilloscope LED1, LED2 wave showed in Figure 9.

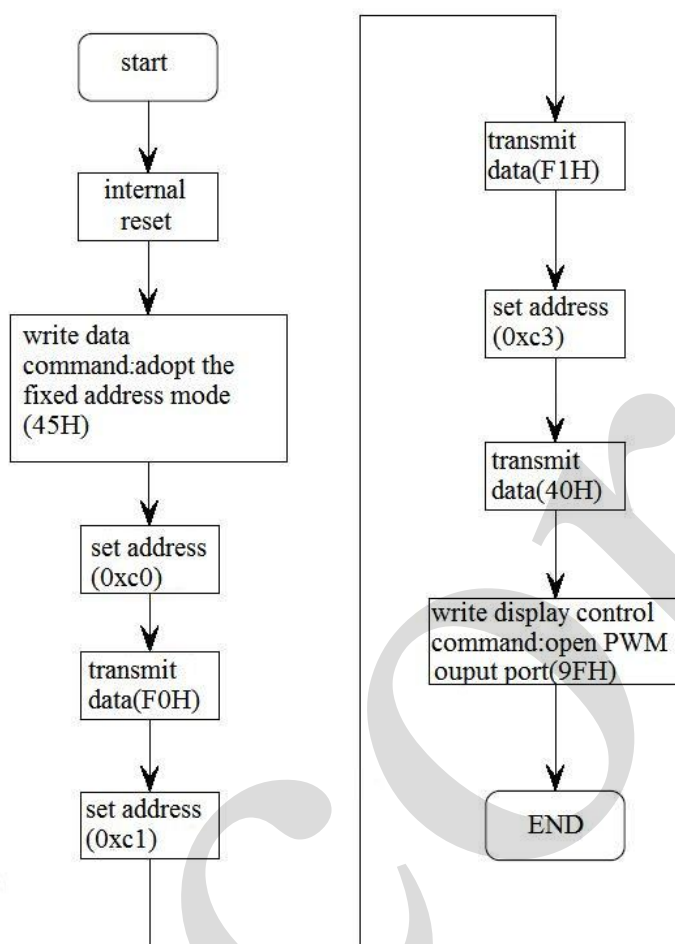


Figure 8 Flowchart of control PWM output port

The wave observed by oscilloscope:

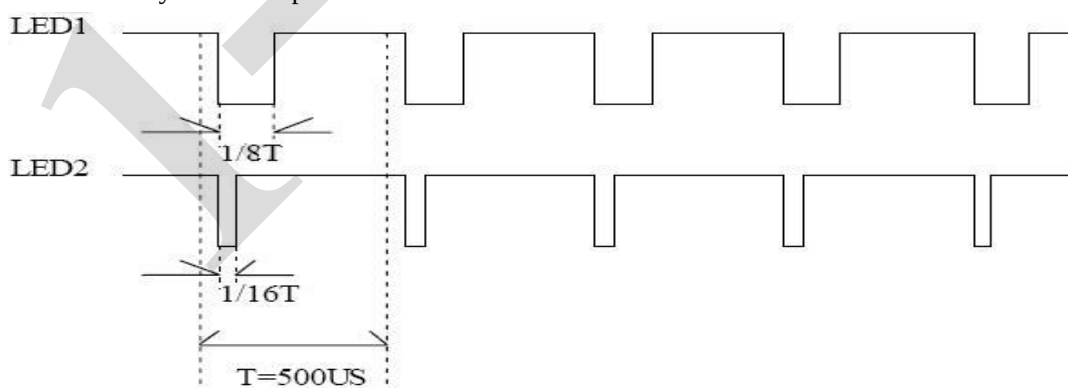


Figure 9



Four PWM outputs are open drain output of N tube. When measured the waveform of LED1-4, the pull-up resistor must be added. LED2 port output waveform is $1/16T$ with reference to FIG. 8. The width is set to T when LED1 writing 0FH in the address C0H. When writing to the address 40H in C3H, the resulting pulse width is $1/8T$ and simple formula given below:

$$t = mn \times T$$

- t Output pulse width, T is a constant (about 500us)
- m Negative Duty set by the LED1, LED2, LED3, LED4 (Low value defining the entire period (T))
- n Negative Duty set by the LED123, LED456 (Low value defining the whole cycle (mT))

4.7.3、Input Port of SW Switching Signal

MCU SW has functions to extend the input port. Similar principles operating SW input port and read the key. Figure 10 is an example to introduce the principle of SW input port.

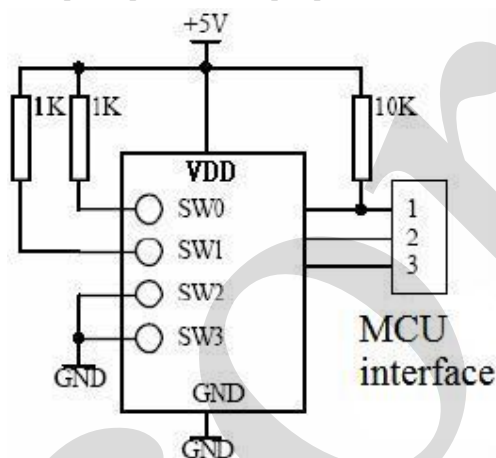


Figure 10

For example, you can read the value is 03H according to the flow of figure 11.

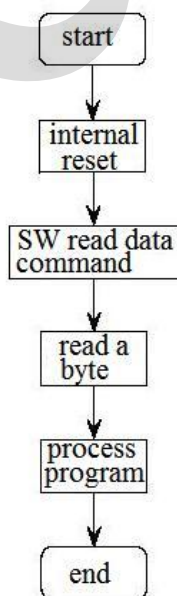
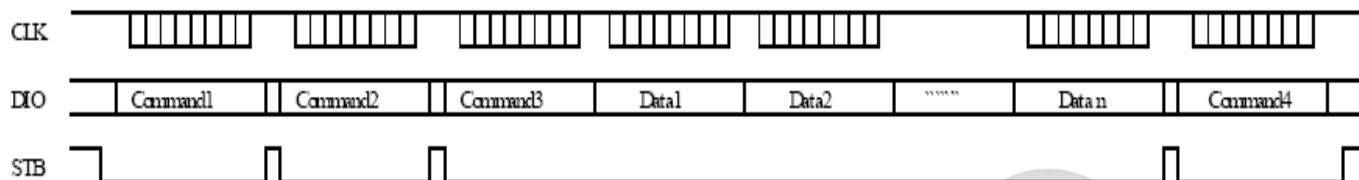


Figure 11

**4.8、Typical Transmission Format Of Serial Data When In Application****4.8.1、Address Add Mode**

Use address auto increment mode, set the address is actually the starting address of the transmitted data stream is stored. Starting Address Command word has been sent, “STB” do not need to set high follow by the transfer of data, most 14BYTE, and data transfer is completed before the “STB” is set high.



Command1: Set Display Mode

Command2: Set Data Command

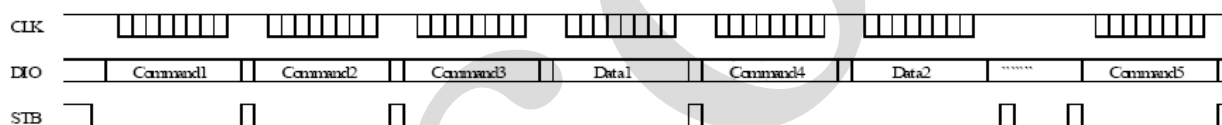
Command3: Set display address

Data1~n: Transmit display data to the Command3 address and the following addresses (Up to 14 bytes)

Command4: Display control command

4.8.2、Fixed Address Mode

Use fixed address mode, set the address which is actually a set of stored data to be transferred 1BYTE. After address been sent, “STB” do not need to set high, 1BYTE data need to transfer followly, and the “STB” is set high when data transfer is completed. Then re-set the address where the second data need to be stored, most 14BYTE data transfer is completed, “STB” is set high at last.



Command1: Set Display Mode

Command2: Set Data Command

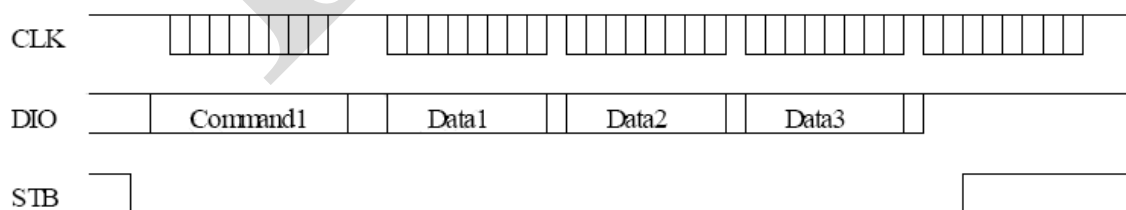
Command3: Set display address 1

Data1: Transmitting display data 1 to the Command3 addresses

Command4: Set display address 2

Data2: Transmitting display data 2 to the Command4 addresses

Command5: Display control command

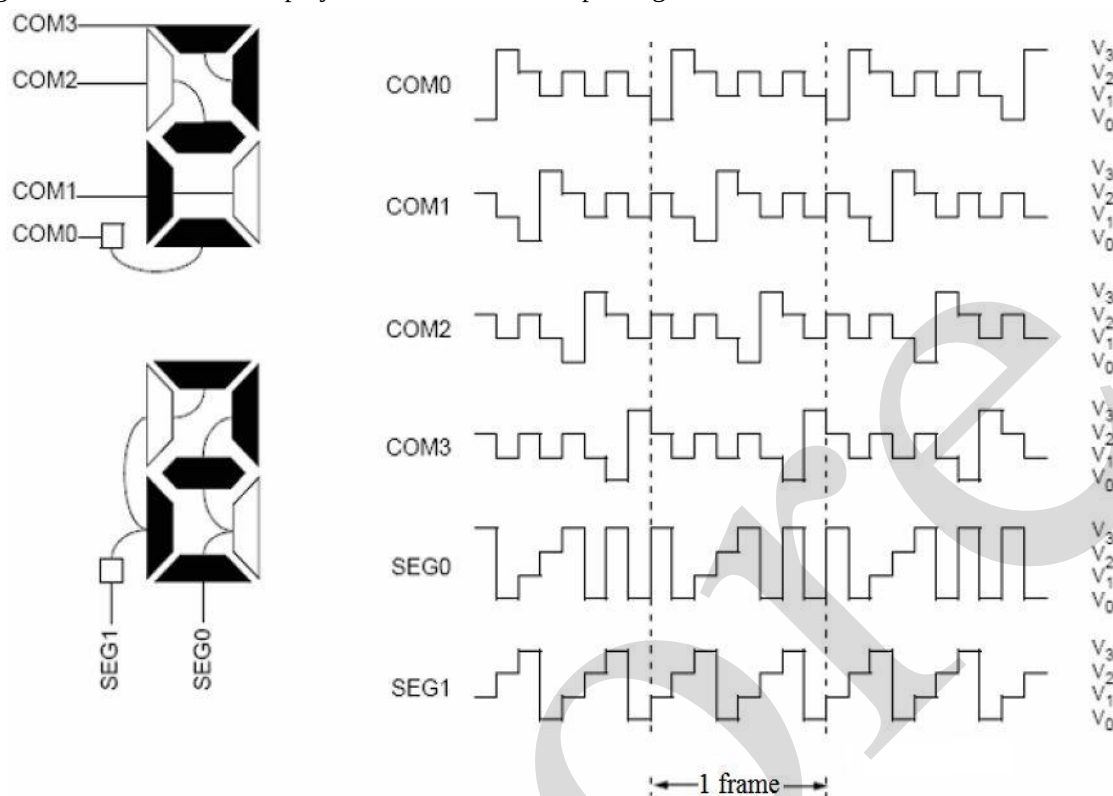
4.8.3、Reading The Key Sequence

Command1: Set Display Mode

Data1~3: Read key data

**4.9、Pin Drive Waveforms**

Using the waveform which displayed “2”,when 1/4 multiplexing and 1/3 bias drive:



$V_3 = V_{DD}$ (V_{DD} supply voltage for the LCD)

$V_2 = 2/3 V_{DD}$

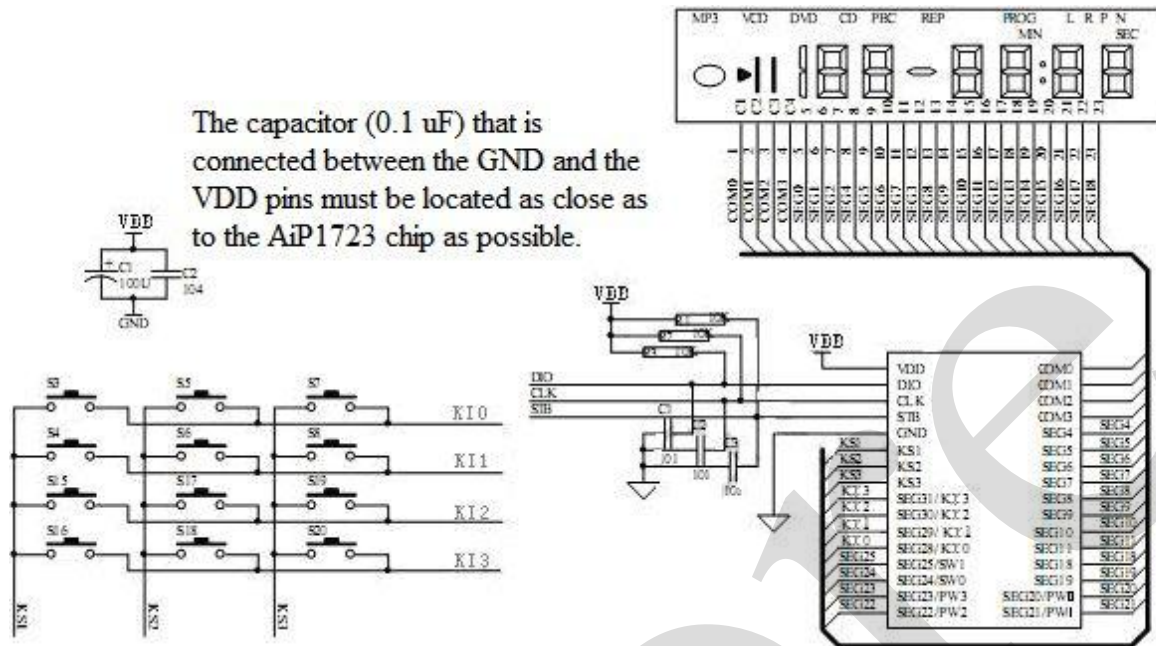
$V_1 = 1/3 V_{DD}$

$V_0 = 0$



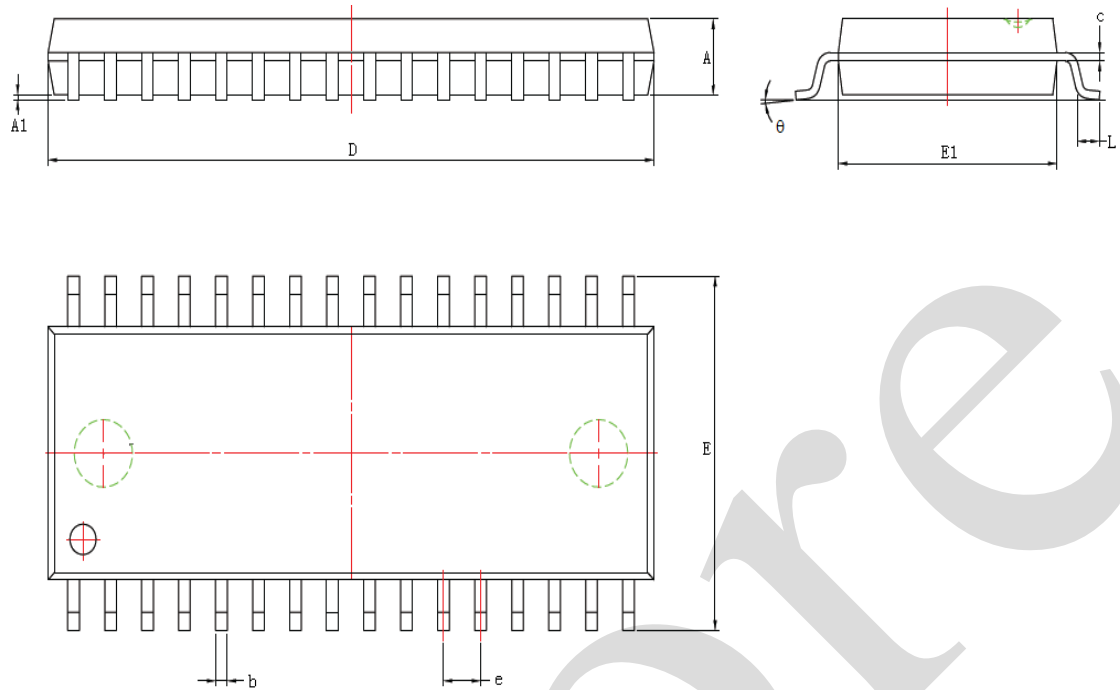
5、Typical Application Circuit And Application Note

5.1、Typical Application Circuit



5.2、Applications Notes

1. In the use of pins of SEG20/PWM0, SEG21/PWM1, SEG22/PWM2, SEG23/PWM3, SEG25/SW1, SEG24/SW0, SEG28/KI0, SEG29/KI1, SEG30/KI2, SEG31/KI3, you can select the second function as needed. Once selected, it can not be switched;
2. Only select 1,2,4 channel PWM pulse width modulation output or PWM function is not used;
3. Only select 2-way general input SW extension or no input port function;
4. Only select 1,2,4 key input port as key scan or don't use key scan function;
5. The filter capacitor between VDD, and GND in the PCB traces should be placed as close as possible AiP1723 chip to enhance the filtering effect;
6. Three 100P capacitors connected to DIO, CLK, STB communication port can reduce interference to the communications port.

**6、Package Information****6.1、SOP32 Package Information**

2023/12/A	Dimensions In Millimeters	
	Min.	Max.
A	2.24	2.59
A1	0.05	0.25
E	10.20	10.60
E1	7.40	7.62
D	20.68	21.08
L	0.55	0.95
e	1.27	
b	0.30	0.50
c	0.25	
θ	0°	8°

**7、Statements And Notes****7.1、The name and content of Hazardous substances or Elements in the product**

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We recommend you to read this chapter carefully before using this product.

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