



AiP1968

3-Line Serial Interface, Common Cathode, 10 Seg×7 Grid or 13 Seg×4 Grid LED Driver and Controller with Ghost Elimination and 10×2 Keyboard input Ports

Product Specification

Specification Revision History:

Version	Date	Description
2018-05-A1	2018-05	New
2024-01-B1	2024-01	Replace the template
2024-08-B2	2024-08	Modify the parameters



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1、General Description

AiP1968 is a 3-line serial interface, common cathode, 10 seg×7 grid or 13 seg×4 grid LED driver and controller with ghost elimination and 10×2 keyboard input ports. It has a built-in 3-line serial communication interface and RC oscillator, with 8-level brightness adjustable. It is widely applied in various LED panel occasions.

Features:

- Display mode software adjustable
- Built-in RC oscillator
- Built-in display RAM
- RAM power-on initialization reset
- 10*2 scanning key matrix
- Built-in ghost elimination function
- Display brightness software adjustable
- 3-line serial interface (CLK, STB, DIO)
- Packing form: SOP24 / SSOP24 (0.635mm)

Application area:

LED display panel occasions, home appliance products such as microwave, induction cooker and water heater



Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP1968SA24.TB	SOP24	AiP1968	30 PCS/tube	80 tube/box	2400 PCS/box	Dimensions of plastic enclosure: 15.4mm×7.5mm Pin spacing: 1.27mm
AiP1968VB24.TB	SSOP24	AiP1968	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 0.635mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP1968SA24.TR	SOP24	AiP1968	1250 PCS/reel	1250 PCS/box	Dimensions of plastic enclosure: 15.4mm×7.5mm Pin spacing: 1.27mm
AiP1968VB24.TR	SSOP24	AiP1968	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 0.635mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Pin Description

2.1、Pin Configurations

1	DIO	GRID1	24
2	CLK	GRID2	23
3	STB	GND	22
4	K1	GRID3	21
5	K2	GRID4	20
6	VDD	SEG14/GRID5	19
7	SEG1/KS1	SEG13/GRID6	18
8	SEG2/KS2	SEG12/GRID7	17
9	SEG3/KS3	SEG10/KS10	16
10	SEG4/KS4	SEG9/KS9	15
11	SEG5/KS5	SEG8/KS8	14
12	SEG6/KS6	SEG7/KS7	13

2.3、Pin Description

Pin No.	Pin Name	I/O	Description
1	DIO	IO	Data port, N-tube open-drain output, built-in pull-up resistance
2	CLK	I	Clock port
3	STB	I	Clip select port
4	K1	I	Key input port, built-in pull-down resistance
5	K2	I	Key input port, built-in pull-down resistance
6	VDD	-	Power supply
7	SEG1/KS1	O	Segment output/key scanning output, P-tube open-drain output
8	SEG2/KS2	O	Segment output/key scanning output, P-tube open-drain output
9	SEG3/KS3	O	Segment output/key scanning output, P-tube open-drain output
10	SEG4/KS4	O	Segment output/key scanning output, P-tube open-drain output
11	SEG5/KS5	O	Segment output/key scanning output, P-tube open-drain output
12	SEG6/KS6	O	Segment output/key scanning output, P-tube open-drain output
13	SEG7/KS7	O	Segment output/key scanning output, P-tube open-drain output
14	SEG8/KS8	O	Segment output/key scanning output, P-tube open-drain output
15	SEG9/KS9	O	Segment output/key scanning output, P-tube open-drain output
16	SEG10/KS10	O	Segment output/key scanning output, P-tube open-drain output
17	SEG12/GRID7	O	Segment/bit multiplexing output, P/N-tube open-drain output
18	SEG13/GRID6	O	Segment/bit multiplexing output, P/N-tube open-drain output
19	SEG14/GRID5	O	Segment/bit multiplexing output, P/N-tube open-drain output
20	GRID4	O	Bit output, N-tube open-drain output
21	GRID3	O	Bit output, N-tube open-drain output
22	GND	-	Ground
23	GRID2	O	Bit output, N-tube open-drain output
24	GRID1	O	Bit output, N-tube open-drain output



3、Electrical Parameter

3.1、Absolute Maximum Ratings

($T_{amb}=25^{\circ}\text{C}$, GND=0V, unless otherwise specified)

Characteristic	Symbol	Conditions	Value	Unit
Power Supply Voltage	VDD	-	-0.5 to +7.0	V
Logic Input Voltage	V_{IN}	-	-0.5 to VDD+0.5	V
Output Pin Break Down Voltage	V_{OBV}	Pulse width<50ns	9.0	V
Output High-Level Drive (SEG)	I_{O1}	-	-50	mA
Output Low-Level Drive (GRID)	I_{O2}	-	+150	mA
Operating Temperature	T_{amb}	-	-40 to +85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-	-65 to +150	$^{\circ}\text{C}$
Soldering Temperature	T_L	10s	260	$^{\circ}\text{C}$

3.2、Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Power Supply Voltage	VDD	3	5	5.5	V
High-Level Input Voltage	V_{IH}	0.7VDD	-	VDD	V
Low-Level Input Voltage	V_{IL}	0	-	0.2VDD	V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(VDD=5V, GND=0V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output High-Level Drive	I_{OH1}	SEG1~SEG14, $V_{OH}=VDD-2V$	-20	-25	-40	mA
	I_{OH2}	SEG1~SEG14, $V_{OH}=VDD-3V$	-20	-30	-50	mA
Output Low-Level Drive	I_{OL1}	GRID1~GRID7, $V_{OL}=0.3V$	80	100	-	mA
	I_{DO}	$V_{OL}=0.4V$, DIO	4	8	-	mA
High-Level Output Current Tolerance	I_{TOLSG}	$V_{OL}=VDD-3V$, SEG1~SEG14	-	-	5	%
Input Leakage Current	I_I	$V_{IN}=VDD$, STB, CLK, DIO	-	-	± 1	uA
		$V_{IN}=GND$, STB, CLK	-	-	± 1	
		$V_{IN}=GND$, DIO	300	500	700	
Input High-Level Voltage	V_{IH}	CLK, DIO, STB	0.7VDD	-	-	V
Input Low-Level Voltage	V_{IL}	CLK, DIO, STB	-	-	0.2VDD	V
Hysteresis Voltage	V_H	CLK, DIO, STB	-	0.35	-	V
Quiescent Current	I_{DD}	No load, $V_{IN}=VDD$	140	160	180	uA
Input Pull-Up Resistance	R_{IP}	DIO	-	10	-	K Ω
Input Pull-Down Resistance	R_L	K1~K2	-	10	-	K Ω



3.3.2、AC Characteristics 1

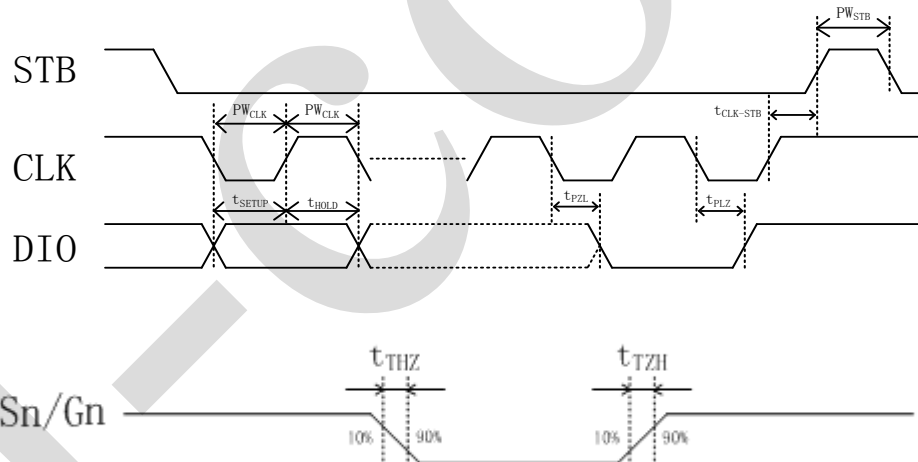
(VDD=4.5V to 5.5V, GND=0V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC}	-	-	400	-	KHz
Transmission Delay Time	t_{PLZ}	CLK→DIO $C_L=15pF, R_L=10K\Omega$	-	-	300	ns
	t_{PZL}		-	-	100	ns
Rise Time	t_{TZH1}	$C_L=300pF$	SEG1~SEG14		2	us
	t_{TZH}		GRID1~GRID7		0.5	us
Fall Time	t_{THZ}	$C_L=300pF, SEGn, GRIDn$		-	120	us
Maximum Clock Frequency	f_{max}	Duty Cycle 50%		1	-	MHz

3.3.3、AC Characteristics 2

(VDD=4.5V to 5.5V, GND=0V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Pulse Width	PW_{CLK}	-	400	-	-	ns
Gate Width	PW_{STB}	-	1	-	-	us
Data Setup Time	T_{setup}	-	100	-	-	ns
Data Retention Time	T_{hold}	-	100	-	-	ns
Clk→stb Time	$T_{clk-stb}$	CLK↑→STB↑	1	-	-	us
Waiting Time	T_{wait}	CLK↑→CLK↓	1	-	-	us





4、Function Description

4.1、Display Register Address

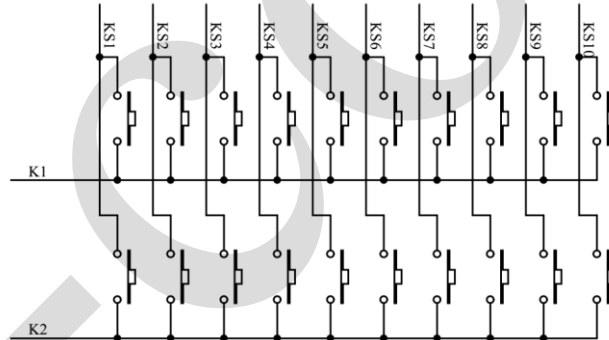
The register stores the data transmitted from the external device to AiP1968 via a serial interface, and the address is assigned as follows:

X	X	SEG14	SEG13	SEG12	X	SEG10	SEG9	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1		
xxHU (High Four)				xxHL (Low Four)				xxHU (High Four)				xxHL (Low Four)					
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0		
01HU				01HL				00HU				00HL				GRID1	
03HU				03HL				02HU				02HL				GRID2	
05HU				05HL				04HU				04HL				GRID3	
07HU				07HL				06HU				06HL				GRID4	
09HU				09HL				08HU				08HL				GRID5	
0BHU				0BHL				0AHU				0AHL				GRID6	
0DHU				0DHL				0CHU				0CHL				GRID7	

Note: There is built-in RAM area power-on initialization reset function in AiP1968 circuit, that is, after power-on the RAM area is displayed as 0 by default.

4.2、Key Scan and Key Scan Data Register

The key scan matrix is 10*2, as shown in the figure below:



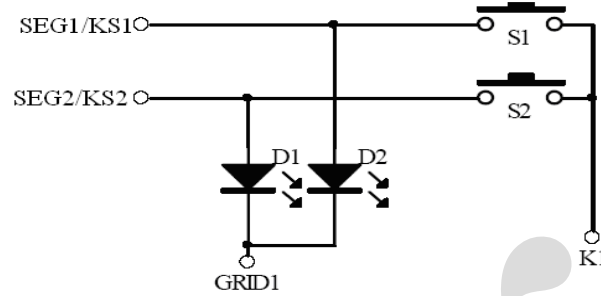
The key scan data storage data is as follows. After running the read key command, read the key data BYTE1-BYTE5 bytes. The read data is output from the low bit, and B6 and B7 bits are invalid bits. When the key corresponding to the K and KS pins of the chip is pressed, the Bit in the corresponding byte is 1.

B0	B1	B2	B3	B4	B5	B6	B7	
K1	K2	X	K1	K2	X	0	0	
KS1			KS2			0	0	BYTE1
KS3			KS4			0	0	BYTE2
KS5			KS6			0	0	BYTE3
KS7			KS8			0	0	BYTE4
KS9			KS10			0	0	BYTE5

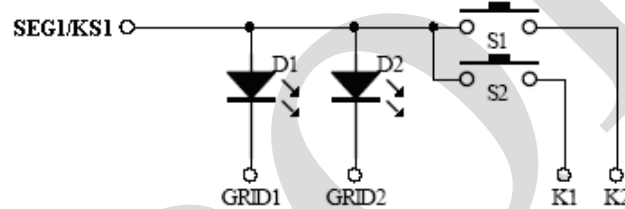


4.2.1、Combination Key

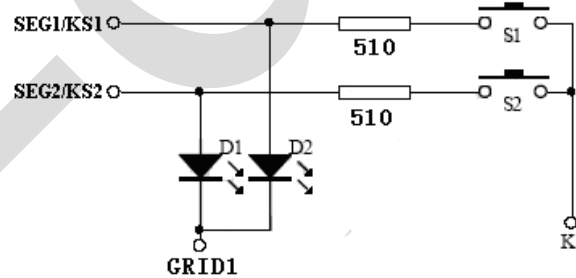
Key scanning is automatically completely by AiP1968, which is not controlled by the user, and the user only needs to read the key value according to the timing. It takes 2 display cycles to complete a key scan, and SEG1/KS1-SEG10/KS10 are multiplex of display and key scan. As shown in the following figure, if D1 is off and D2 is on, set SEG1 to 1 and SEG2 to 0. If S1 and S2 are pressed at the same time, SEG1 and SEG2 are short-circuited. In this case, both D1 and D2 are lit, resulting in abnormal display. When you need to use a combination of keys, there are a few things to pay attention to:



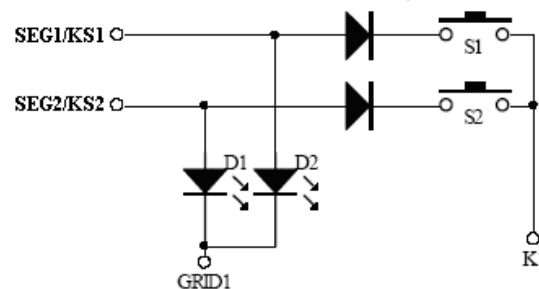
1. On the hardware, the keys that need to be pressed at the same time can be set on different K-lines, as shown in the figure below.



2. Install the resistance in series on SEG1-SEGN. The resistance value of the resistance should be selected at 510 ohms. If the value is too large, it will cause the key to lose efficiency; if the value is too small, it may fail to solve the problem of display interference, as shown in the figure below:



3. Install the diodes in series on SEG1-SEGN, as shown in the figure below.





4.3、Instruction Introduction

Each time the STB port changes from high to low, the first byte sent into the circuit from the DIO port is used as an introduction input, and the second byte is used as a data input. The higher two digits in an instruction are used to distinguish between different instructions.

B7	B6	Instruction
0	0	Display mode setting
0	1	Data command setting
1	0	Display control command setting
1	1	Address command setting

If STB is set to high during instruction or data transmission, serial communication is initialized and the instruction or data being transmitted is invalid (the previously transmitted instruction or data remains valid).

4.3.1、Display Mode Setting

This command is used to set the number of selected driver segments and bits. When the command is executed, the display is forcibly closed. To redisplay, the display ON/OFF instruction “ON” must be executed, but this does not happen when the same mode is set.

MSB				LSB				Display Mode
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	Irrelevant term, write 0				0	0	4grid 13seg
0	0					0	1	5grid 12seg
0	0					1	0	6grid 11seg
0	0					1	1	7grid 10seg

Note: The default display mode of AiP1968 is 7grid 10seg.

4.3.2、Data Setting

This instruction is used to set data reading and writing. B1 and B0 cannot be set to 01 and 11.

MSB				LSB				Function	Description
B7	B6	B5	B4	B3	B2	B1	B0		
0	1	Irrelevant term, write 0		-	-	0	0	Read-write mode setting	Write data to the display register
0	1			-	-	1	0		Read the key value
0	1			-	0	-	-	Address mode setting	Address auto-adding mode
0	1			-	1	-	-		Fixed address mode
0	1			0	-	-	-	Test mode setting	Normal mode
0	1			1	-	-	-		Test mode (internal use)



4.3.3、Address setting

This instruction is used to set the address of the display register. If the address is set higher than 0DH, the data is ignored until the effective address is set.

MSB

LSB

B7	B6	B5	B4	B3	B2	B1	B0	Display Address
1	1	Irrelevant term, write 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH

4.3.4、Display Control

This instruction is used to set the display switch and display brightness adjustment. There exist a total of eight levels of brightness to be adjusted in the circuit.

MSB

LSB

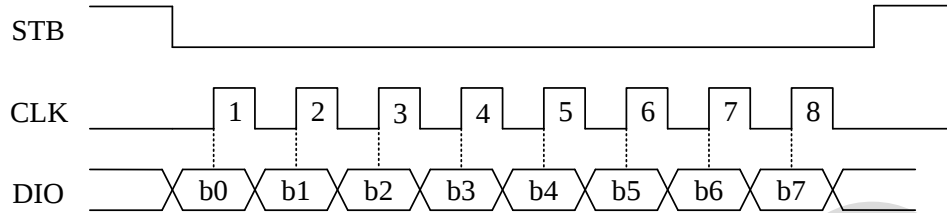
B7	B6	B5	B4	B3	B2	B1	B0	功能	说明
1	0	Irrelevant term, write 0		-	0	0	0	Display brightness setting	Set the pulse width to 1/16
1	0			-	0	0	1		Set the pulse width to 2/16
1	0			-	0	1	0		Set the pulse width to 4/16
1	0			-	0	1	1		Set the pulse width to 10/16
1	0			-	1	0	0		Set the pulse width to 11/16
1	0			-	1	0	1		Set the pulse width to 12/16
1	0			-	1	1	0		Set the pulse width to 13/16
1	0			-	1	1	1		Set the pulse width to 14/16
1	0			0	-	-	-	Display switch setting	Display off
1	0			1	-	-	-		Display on



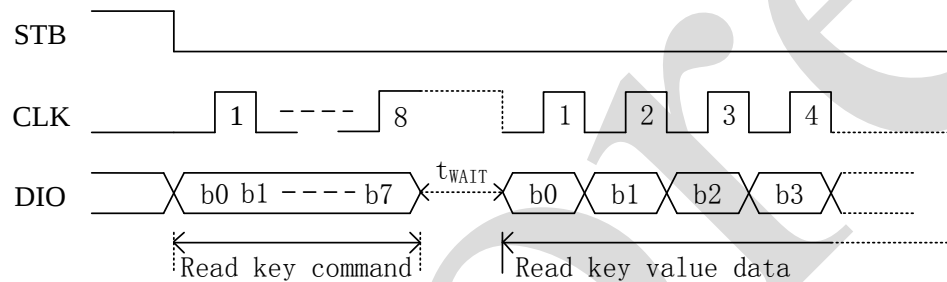
4.4、Serial Data Transmission Format

Both reading and receiving 1 bit operate on the rising edge of the clock.

4.4.1、Write Data



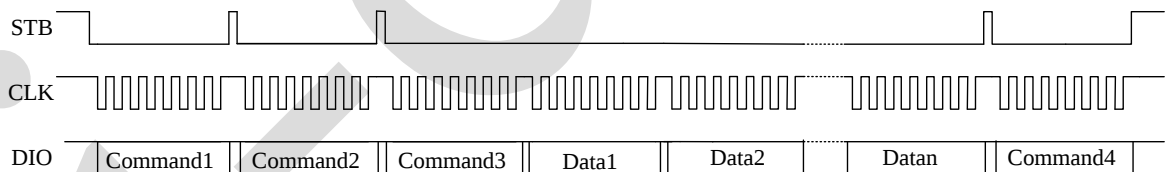
4.4.2、Read Data



Note: When reading data, a waiting period t_{WAIT} (min. 1us) is required between setting the instruction at the beginning of the 8th rising edge of the serial clock CLK and reading the data at the falling edge of CLK.

4.5、Transmission of Serial Data in Application

4.5.1、Address Increment Mode Communication Timing



Command1: Set display mode

Command2: Set data instruction

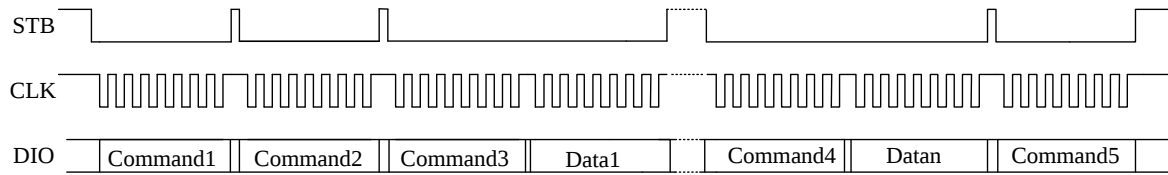
Command3: Set display address

Data1~Datan: Transmit display data

Command4: Display control instruction

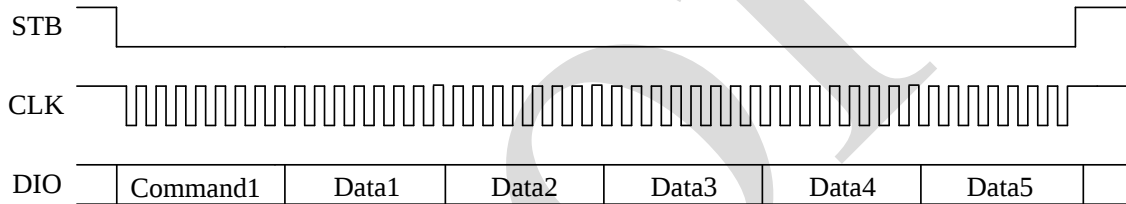


4.5.2、Fixed Address Mode Communication Timing

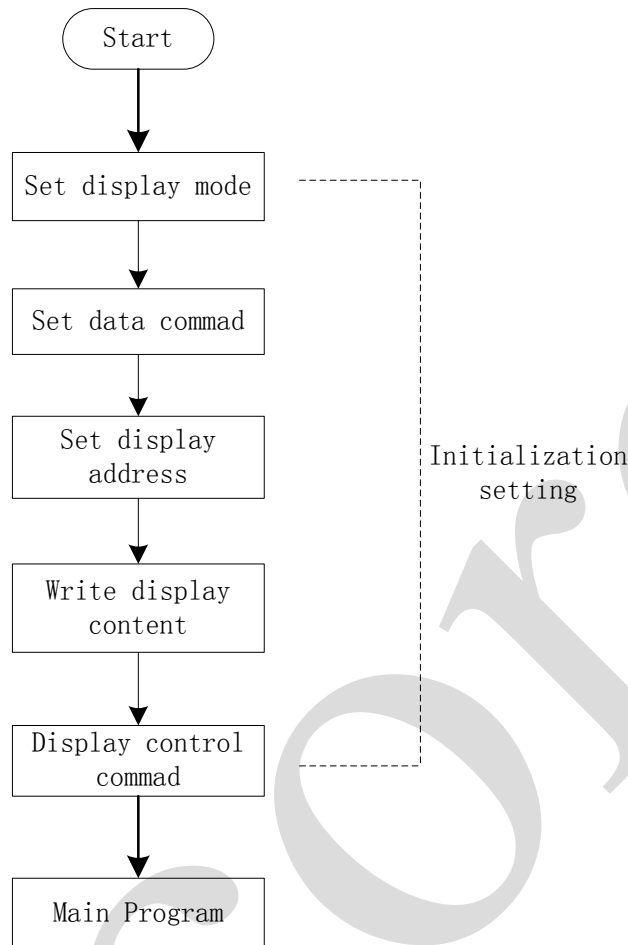


Command1: Set display mode
Command2: Set data instruction
Command3: Set display address 1
Data1: Display data written into Command3 address
⋮
Command4: Set display address N
Datan: Display data written into Command4 address
Command5: Display control instruction

4.5.3、Read Key Value Timing



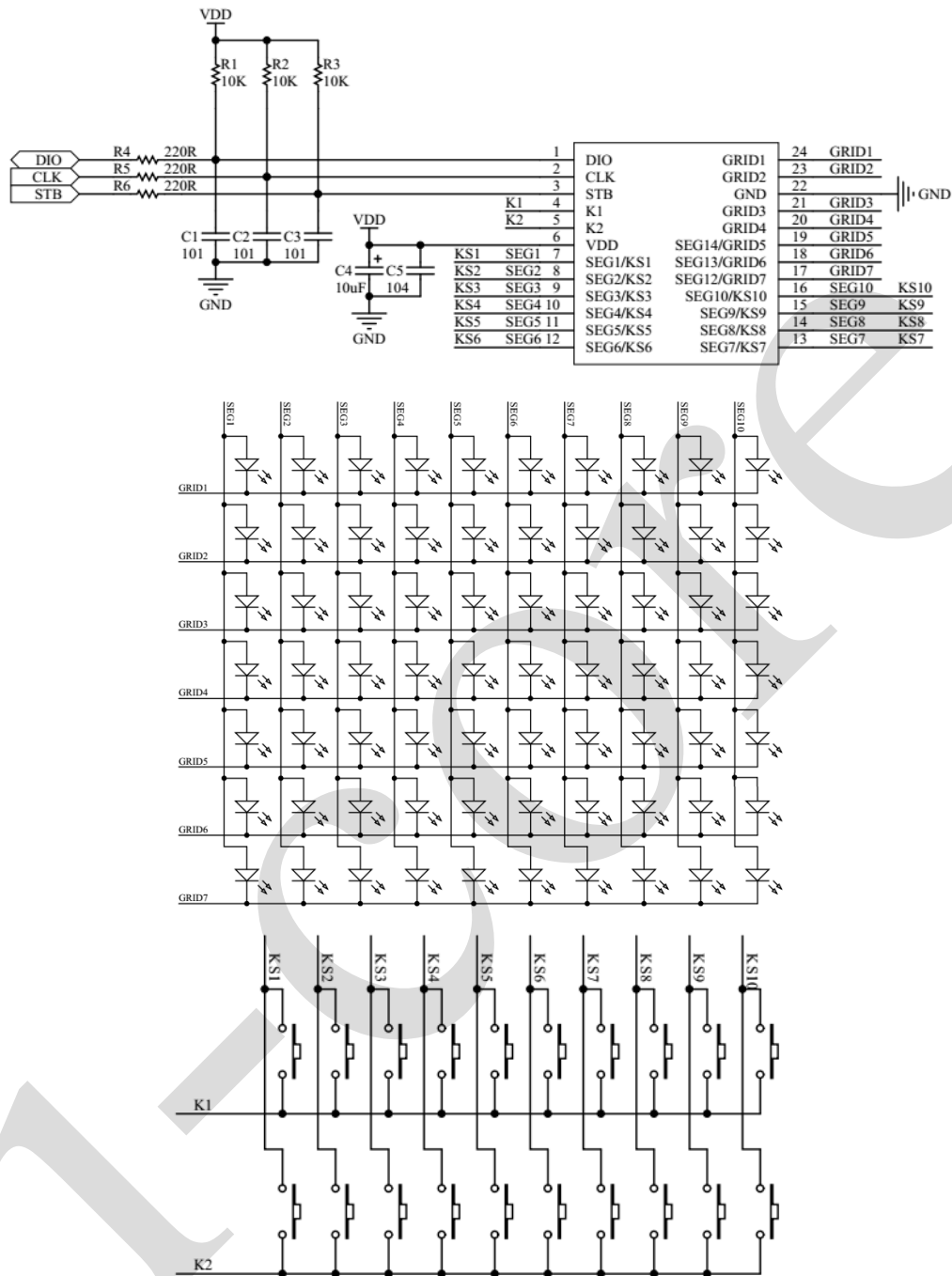
Command1: Set read key instruction
Data1~5: Key value data that is read

**4.6、Initialization Flowchart****Note:**

1. The display mode setting is used to select the number of segments to drive the display screen, which needs to be selected according to the actual hardware connection of the user. Generally, it is only set in the initialization part. The default display mode for AiP1968 is 7grid 10seg.
2. The data instruction is used to choose whether to write the display data to the RAM area (which is divided into fixed address and address auto-adding) or to read the key value.
3. AiP1968 circuit has built-in RAM function of power-on clearing. If the user directly turned on the display without writing the display data, then there is no display.
4. AiP1968 has built-in function of ghost elimination, which can prevent the brightness issue.



5、Typical Application Circuit



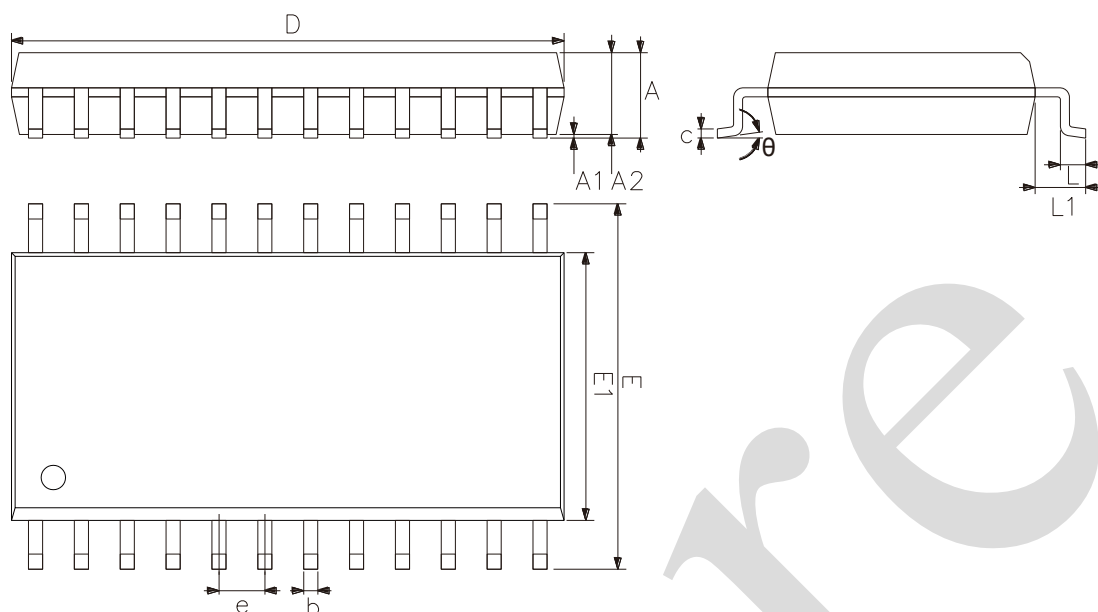
Note:

1. The filtering capacitor between VDD and GND should be close to AiP1968 to enhance the filtering effect.
2. In order to improve the anti-interference ability of the circuit, it is recommended to connect the communication port according to the figure above, and the specific parameter values can be adjusted according to the actual needs.



6、Package Information

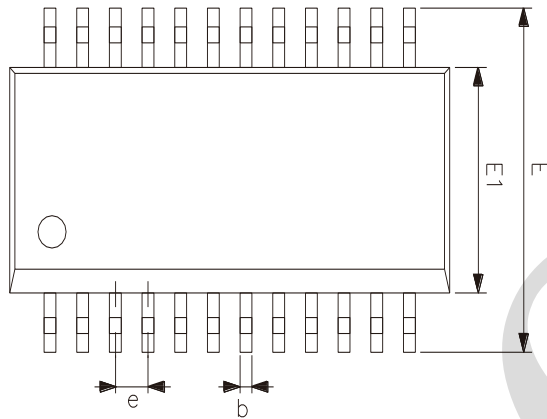
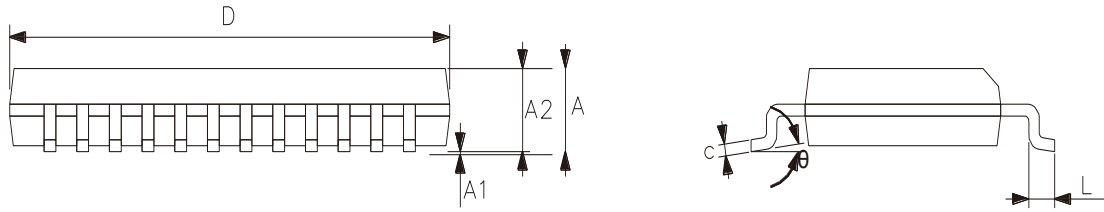
6.1、SOP24



2023/12/A	Dimensions In Millimeters	
Symbol	Min.	Max.
A	2.35	2.65
A1	0.10	0.30
A2	2.13	2.44
b	0.39	0.47
c	0.25	0.30
D	15.19	15.55
E	10.10	10.57
E1	7.40	7.62
e	1.27	
L	0.41	1.00
L1	1.30	1.50
θ	0°	8°



6.2、SSOP24 (0.635mm)



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.30	1.55
b	0.23	0.47
c	0.19	0.26
D	8.45	8.85
E	5.80	6.20
E1	3.70	4.10
e	0.635	
L	0.40	0.80
θ	0°	8°



7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests i-Core's application to avoid failure in the application or the application of the customer's third party users. I-Core does not accept any liability.

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