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AiP3331

Audio Modulated, double Matrix Scan Driver and Controller for 8×9 Dots Matrix LED with Constant Current

Product specification

Manual release resume:

Version	Date	Description
2023-08-A1	2023-08	New
2023-08-A2	2023-08	Update the recommended information of REXT
2024-06-A3	2024-06	Modify the content



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1, General Description

AiP3331 is a dot matrix LED drive controller, which can drive two groups of LED arrays in a constant current mode, and each group of LED arrays consists of 72 monochromatic LEDs at most.

AiP3331 can perform 256-step linear dimming on each LED. The circuit can store up to 8 frames of display graphics information, and the output graphics can be selected by external audio signals.

Its main features are as follows:

- \bullet Driving lattice size: 2 groups \times 72 LED lattice.
- Constant current drive
 Adjust the current of constant current drive through peripheral resistance.
- Built-in display data memory (DDRAM)
 Can store 8 frames of pictures.
- Rich display effect control

Independent switch control at each point.

Independent flicker control at each point

Independent 256-order PWM brightness control at each point

Choose static picture display or automatic playback mode.

Choose the breathing mode that is automatically controlled when switching images.

The image frame number can be controlled using audio signal input.

Image brightness can be controlled using audio signal input.

- communication interface: I ² C interface.
- operating voltage is 2.7V to 5.5V
- package information: QFN28/SSOP28/ESSOP28.

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Order information:

Pipe installation:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Remarks
AiP3331VB28.TB	SSOP28	AiP3331	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 9.8mm×3.8mm Pin spacing: 0.635mm
AiP3331VE28.TB	ESSOP28	AiP3331	50 PCS/tube	100 tube/box	5000 PCS/box	Dimensions of plastic enclosure: 9.8mm×3.8mm Pin spacing: 0.635mm
AiP3331QB28.TB	QFN28	AiP3331	490 PCS/plate	10 plate/box	4900 PCS/box	Dimensions of plastic enclosure: 4.0mm×4.0mm Pin spacing: 0.40mm

Braiding:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Remarks
AiP3331VB28.TR	SSOP28	AiP3331	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 9.8mm×3.8mm Pin spacing: 0.635mm
AiP3331QB28.TR	QFN28	AiP3331	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 4.0mm×4.0mm Pin spacing: 0.40mm
AiP3331VE28.TR	ESSOP28	AiP3331	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 9.8mm×3.8mm Pin spacing: 0.635mm

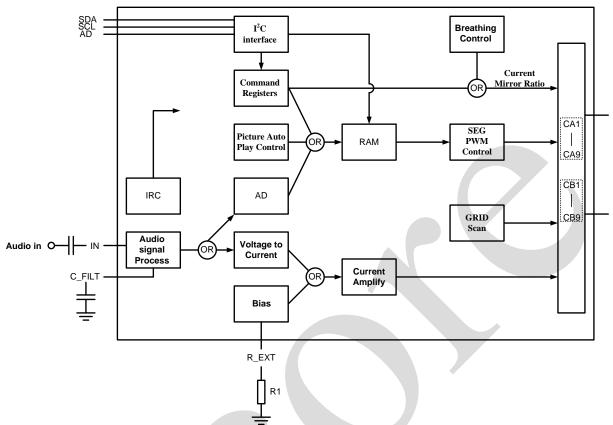
Note: If the material object is inconsistent with the ordering information, please take the material object as the standard.



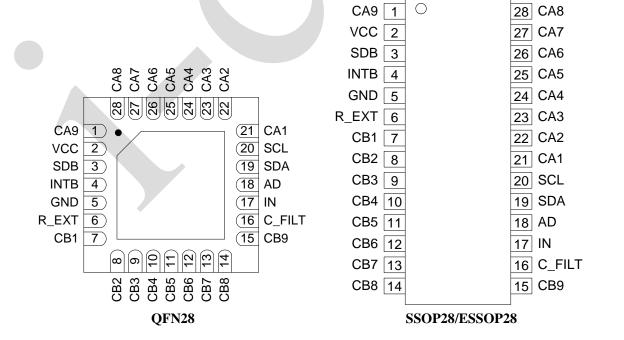
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2, Block Diagram And Pin Description

2.1 Block Diagram



2.2, Pin Configurations





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2.3 Pin Description

Pin Name	Ю	Description
VCC	supply electricity	Power Supply
GND	supply electricity	land
CA1 to CA9	О	LED driving output GRID/SEG
CB1 to CB9	О	LED driving output GRID/SEG
SDA	IO	Communication interface data terminal
SCL	I	Communication interface clock end
AD	I	Communication interface address selection end
SDB	I	Reset signal input
INTB	0	Interrupt signal output
IN	I	Audio signal input end
R_EXT	О	Driving current control terminal
C_FILT	0	Audio signal filtering

3, Electrical Parameter

3.1. Absolute Maximum Ratings

 $T_{amb}=25$ °C, unless otherwise specified

Characteristic	Symbol	Conditions	Value	Unit
Power supply voltage	VCC	-	-0.3 to +6.0	V
MAX Power supply current	ICC	·	720	mA
input voltage	VIN	-	-0.3 to VCC+0.3	V
operating ambient temperature	T_{amb}	-	-40 to +85	$^{\circ}$
storage temperature	T_{stg}	-	-65 to +150	$^{\circ}\!\mathbb{C}$
welding temperature	$T_{ m L}$	10s	260	$^{\circ}\!\mathbb{C}$

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3.2, Electrical Characteristics

3.2.1 DC Characteristics

(T_{amb} =25 °C, VCC=3.6V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
operating voltage	VCC	-	2.7	-	5.5	V
operational current	I_{CC}	V _{IN} =0V, no audio input. All LED off	-	2.17	-	mA
		V _{SDB} =0V	-	0.5	5	
Turn-off current	I_{SD}	V _{SDB} =VCC Software shutdown mode 1	-	230	350	uA
Output constant current CA1 to CA9 CB1 to CB9	I_{OUT}	Automatic control current No audio signal input R_{EXT} =20 $K\Omega$	-	34[1]	-	mA
Output voltage CA1 to CA9	$ m V_{HR}$	Output high level Constant current =34mA		VCC-0.4		V
CB1 to CB9		Output low level Current =270mA ^[1]	-	0.4	-	V
scanning time	T_{S}	-	-	106	-	us
Non overlapping time	T_{SOL}	-	-	15	-	us
Output average current	I_{LED}	R _{EXT} =20KΩ Maximum PWM duty cycle ^[2]	-	3.2	-	mA
High level input voltage	V_{IH}	VCC=3.6V	0.75*VCC	1	VCC	V
Low level input voltage	$V_{\rm IL}$	VCC=3.6V	GND	-	0.25*VCC	V
High level input leakage	I_{IH}	V _{IN} =V _{IO}	-	5	-	nA
Low level input leakage	$I_{\Pi L}$	V _{IN} =GND	-	5	-	nA

Note:

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^[1] all LEDs are turned on.

^[2] I $_{LED}$ = 64.7/R $_{EXT}$. The recommended range of R_{EXT} is $18K\Omega \sim 25K\Omega$. The minimum value is $10K\Omega$.



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3.3.2, AC Characteristics

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Serial communication frequency	PSR_{CL}	-	-	1	1	MHz
Bus idle time	t_{BUF}	-	-	0.5	-	us
Start flag holding time	t _{HD} , _{STA}	-	-	0.26	-	us
Setup time of restart state	t_{SU} , $_{STA}$	-	-	0.26	-	us
Stop flag setup time	t_{SU} , sto	-	-	0.26	-	us
Data retention time	t_{HD} , $_{DAT}$	-	-	0	-	us
Data setup time	$t_{SU,\ DAT}$	-	-	50	-	ns
SCL low level time	t_{LOW}	-	-	0.5	,	us
SCL high time	t_{HIGH}	-	-	0.26	-	us
Rising time of SDA and SCL	t_R	_[1]	-	20+0.1C _b	300	ns
SDA, SCL falling time	t_{F}	_[1]	-	20+0.1C _b	300	ns

Note:

[1] C $_b$ = total parasitic capacitance on the bus, pF level. I $_{SINK}$ (6mA,t $_R$ and t $_F$ measured signals change from 0.3×VCC to 0.7×VCC.

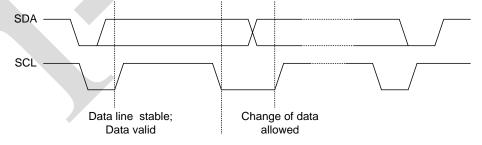
4. Function Description

4.1, I²C Serial Interface

This chip provides a standard I ²C serial interface, and it is only used as a slave for I ²C communication. Two-way two-wire communication can be carried out in different IC or modules, that is, a serial data line SDA and a serial clock line SCL. These two wires are respectively connected to the positive power supply through a pull-up resistor with a typical value of 4.7 k. When I ²C bus is idle, both lines are high. The microcontroller connected with I ²C interface must be open drain or open collector output to realize the wired-or function. Only when I ²C interface is idle will data transmission be started.

4.2. The Validity Of Data

During SCL=1, the data bits at the SDA pin must remain stable. Only when SCL=0, the level of SDA pin is allowed to change, as shown in the following figure:

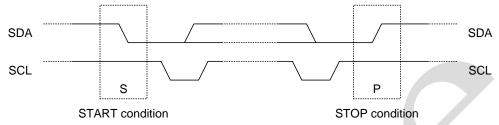




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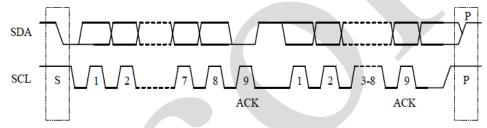
4.3, START and STOP Conditions

- During SCL=1, if SDA changes from high to low, it is indicated as a START signal.
- During SCL=1, if SDA changes from low to high, it is indicated as a STOP signal.
- START and STOP signals are always sent by the host. After the START signal is issued, the I ²C bus is considered to be in a busy state. After the STOP signal is sent out, I 2C bus is considered to be idle again for a period of time.



4.4. Byte Format

Each byte on the SDA line must be 8 bits long. There is no limit to the number of bytes that can be transmitted at a time. Each byte must be followed by an answer bit. Data transmission starts from the most significant bit.



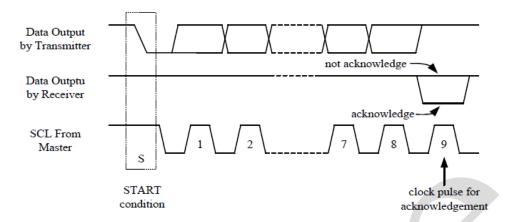
4.5, Acknowledge (ACK)

- Every 8-bit byte is followed by a reply signal. The response signal is the low level sent by the receiver to the I²C bus. The host generates an additional correlated response clock pulse signal.
- The slave with matching address must generate an ACK response signal after receiving each byte.
- The equipment that sends the reply signal must pull SDA low during the reply clock pulse and keep it low during the reply clock pulse high.
- The receiver of the master generates a NACK signal when the slave sends the last byte to inform the slave to end data transmission. In this case, the host receiver must make the data line high during the ninth clock pulse to indicate no answer. The host will generate a STOP signal or repeat the START signal.

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4.6. Slave Address

- After the master sends the START signal, the first thing it receives is the slave address byte. The first seven bits of the first byte are the slave address, and the eighth bit is the read/write bit. When A0 is "1", select read operation; When it is "0", select the write operation.
- The slave address of AIP3331 is affected by the status of AD port:

place	A7~A3	A2~A1	A0
set value	11101	AD	0/1

AD = 00 when ad is connected to GND;

When AD is connected to VCC, AD=11;

AD = 01 when connecting SCL;

AD = 10 when connecting SDA.

4.7 Register Address Self-adding Function

When writing data to AiP3331, you need to set the target address of the data. After AiP3331 receives the data and returns the ACK signal, the internal address pointer will be automatically incremented by 1. This enables AiP3331 to write data of continuous addresses in a START~STOP cycle.

4.8 Read Register

AiP3331 can read the data of internal registers through IIC interface:

- 1. The page address register (address 0xFD) is unreadable.
- 2. The function register (address 0x00~0x0C) can be read.
- 3. The frame data register (address $0x00\sim0xB3$) can only be read when the software is off and SDB = H.

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4.9、Register

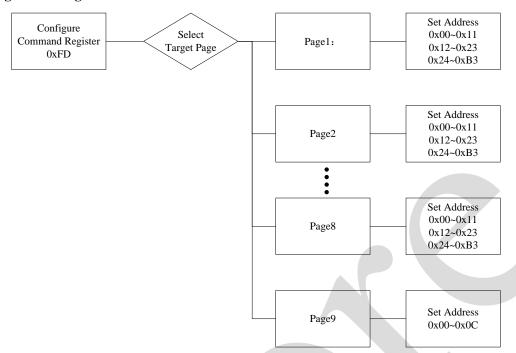
Address	Name	Function	R/W	
	Pag	ge address register		
0xFD	Page address register	Specifies that the address pointer points to	W	
	Frame data	a registers (Page1~Page8)		
0x00~0x11	LED switch control register	Store the switch state of each LED.		
0x12~0x23	Flashing switch control register	Storing the blinking function state of each LED.	R/W	
0x24~0xB3	PWM dimming control register	Storing lighting duty ratio data of each LED.		
	Funct	tion register (Page9)		
0x00	Mode selection register	Configure operation mode	R/W	
0x01	Picture selection register	Select the number of the displayed picture.	R/W	
0x02	Auto Play Settings Register 1	Set the number of autoplay and picture number.	R/W	
0x03	Auto Play Settings Register 2	Set the automatic playback switching picture time.	R/W	
0x04	NC	Reserved bit	R/W	
0x05	Display setting register	Set the display function	R/W	
0x06	Audio synchronization setting register	Audio mode on/off	R/W	
0x07	Frame number register	Read the display picture number	R	
0x08	Respiratory effect control register 1	Set the automatic breathing mode fade-in and fade-out time	R/W	
0x09	Respiratory effect control register 2	Set the automatic breathing mode fade-in and fade-out period.	R/W	
0x0A	Software shutdown control register	Set shutdown mode	R/W	
0x0B	Audio control register 1	Audio mode setting 1	R/W	
0x0C	Audio control register 2	Audio mode setting 2	R/W	
		· ·		

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4.10 Register Configuration Process



4.11, Page Address Register (address 0xFD)

data	function	data	function
0000 0000	Point to Page1 (frame 1 data register)	0000 0001	Point to Page2 (frame 2 data register)
0000 0010	Point to Page3 (frame 3 data register)	0000 0011	Point to Page4 (frame 4 data register)
0000 0100	Point to Page5 (frame 5 data register)	0000 0101	Point to Page6 (frame 6 data register)
0000 0110	Point to Page7 (Frame 7 data register)	0000 0111	Point to Page8 (frame 8 data register)
0000 1011	Point to Page9 (function register)		

4.12. Frame Data Register

4.12.1. Address 00h~11h (LED switch control register)

place	D7	D6	D5	D4	D3	D2	D1	D0
name	C_{M-8}	C _{M-7}	C_{M-6}	C_{M-5}	C_{M-4}	C_{M-3}	C_{M-2}	C_{M-1}
Reset value	X	X	X	X	X	X	X	X

The LED control register is used to store the switch state of each LED in the lattice.

$$\begin{split} &C_{M\text{-}N} = \!\! 0 & \text{Corresponding LED off} \\ &C_{M\text{-}N} = \!\! 1 & \text{Corresponding LED on} \end{split}$$

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4.12.2, Address 12h~23h (flashing switch control register)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name	C_{M-8}	C _{M-7}	C_{M-6}	C_{M-5}	C_{M-4}	C_{M-3}	C_{M-2}	C_{M-1}	_

The flicker control register is used to store the flicker function switch of each LED in the lattice.

 $C_{M\text{-}N}$ =0 Corresponding LED flashing off $C_{M\text{-}N}$ =1 The corresponding LED flashes on.

4.12.3, Address 24h~B3h(PWM dimming control register)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name	D7	D6	D5	D4	D3	D2	D1	D0	_

The PWM duty ratio register is used to store the duty ratio of each LED lighting time in the lattice. Each LED point has 256 steps of duty cycle control. The output current of each LED can be calculated by the following formula

$$I_{PWM} = \frac{D[7:0]}{256} \bullet IMAX$$

D7:D0 should not be set to 0x01.

For example, D7:D0=0xF0 (decimal 240), then the output current is

$$I_{PWM}=IMAX\times240/256$$

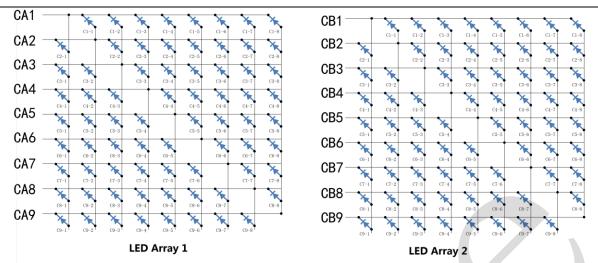
In the formula, IMAX is controlled by the resistance of R_EXT port.

4.12.4. Frame Data Register Address

	LED position	on-off control Register address	Scintillation control Register address	PWM Register address
	CA1 _(C1-1~C1-8)	0x00	0x12	0x24∼0x2B
	CA2 _(C2-1~C2-8)	0x02	0x14	$0x34\sim0x3B$
	CA3 _(C3-1~C3-8)	0x04	0x16	0x44∼0x4B
	CA4 _(C4-1~C4-8)	0x06	0x18	0x54∼0x5B
Lattice 1	CA5 _(C5-1~C5-8)	0x08	0x1A	0x64∼0x6B
	CA6 _(C6-1~C6-8)	0x0A	0x1C	$0x74\sim0x7B$
	CA7 _(C7-1~C7-8)	0x0C	0x1E	0x84∼0x8B
	CA8 _(C8-1~C8-8)	0x0E	0x20	0x94∼0x9B
	CA9 _(C9-1~C9-8)	0x10	0x22	$0xA4\sim 0xAB$
	CB1 _(C1-1~C1-8)	0x01	0x13	0x2C~0x33
	CB2 _(C2-1~C2-8)	0x03	0x15	0x3C∼0x43
	CB3 _(C3-1~C3-8)	0x05	0x17	0x4C~0x53
	CB4 _(C4-1~C4-8)	0x07	0x19	0x5C~0x63
Lattice 2	CB5 _(C5-1~C5-8)	0x09	0x1B	0x6C~0x73
	CB6 _(C6-1~C6-8)	0x0B	0x1D	0x7C~0x83
	CB7 _(C7-1~C7-8)	0x0D	0x1F	0x8C~0x93
	CB8 _(C8-1~C8-8)	0x0F	0x21	0x9C∼0xA3
	CB9 _(C9-1~C9-8)	0x11	0x23	0xAC∼0xB3



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4.13, Function Register

4.13.1, Address 00h (mode selection register)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name	0 (R)	1 (R)	_	MC	DDE		PSR		0x40

MODE= MODE= MODE=	00 01 10/11	Picture mode Automatic playback mode Audio synchronization mode
PSR=	000	In autoplay mode, the starting frame is the first frame.
PSR=	001	In autoplay mode, the starting frame is frame 2.
PSR=	010	In autoplay mode, the starting frame is frame 3.
PSR=	011	In autoplay mode, the starting frame is frame 4.
PSR=	100	In autoplay mode, the starting frame is frame 5.
PSR=	101	In autoplay mode, the starting frame is frame 6.
PSR=	110	In autoplay mode, the starting frame is frame 7.
PSR=	111	In autoplay mode, the starting frame is frame 8.

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4.13.2, Address 01h (picture selection register)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name			_				PSR		0x00

PSR=	000	In picture mode, frame 1 is displayed.
PSR=	001	In picture mode, frame 2 is displayed.
PSR=	010	In picture mode, frame 3 is displayed.
PSR=	011	In picture mode, frame 4 is displayed.
PSR=	100	In picture mode, frame 5 is displayed.
PSR=	101	In picture mode, frame 6 is displayed.
PSR=	110	In picture mode, frame 7 is displayed.
PSR =	111	In picture mode, frame 8 is displayed.

4.13.3、Address 02h (Auto Play Setting Register 1)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name			LOOP		_		NUM		0x00

LOOP=	000	In the automatic playback mode, the whole playback is repeated continuously.
LOOP=	001	In the automatic playback mode, the whole playback is repeated once and then stopped.
LOOP=	010	In the automatic playback mode, the whole playback is repeated twice and then stopped.
LOOP=	011	In the automatic playback mode, the whole playback is repeated 3 times and then stopped.
LOOP=	100	In the automatic playback mode, the whole playback is repeated 4 times and then stopped.
LOOP=	101	In the automatic playback mode, the whole playback is repeated 5 times and then stopped.
LOOP=	110	In the automatic playback mode, the whole playback is repeated 6 times and then stopped.
LOOP=	111	In the automatic playback mode, the whole playback is repeated 7 times and then stopped.
NUM=	000	In autoplay mode, all frames of graphics are played continuously.
NUM=	001	In automatic playback mode, one frame of graphics is played continuously.
NUM=		
INOIVI—	010	In automatic playback mode, 2 frames of graphics are played continuously.
NUM=	010 011	In automatic playback mode, 2 frames of graphics are played
		In automatic playback mode, 2 frames of graphics are played continuously. In automatic playback mode, 3 frames of graphics are played
NUM=	011 100	In automatic playback mode, 2 frames of graphics are played continuously. In automatic playback mode, 3 frames of graphics are played continuously. In automatic playback mode, 4 frames of graphics are played continuously.
NUM=	011	In automatic playback mode, 2 frames of graphics are played continuously. In automatic playback mode, 3 frames of graphics are played continuously. In automatic playback mode, 4 frames of graphics are played continuously. In autoplay mode, 5 frames of graphics are played continuously.
NUM=	011 100	In automatic playback mode, 2 frames of graphics are played continuously. In automatic playback mode, 3 frames of graphics are played continuously. In automatic playback mode, 4 frames of graphics are played continuously.

Playback will stop on the graph of the next frame corresponding to the set value. For example,

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PSR=011,LOOP=011,NUM=011, then the picture will be played three times between the 4th and 6th frames, and then stop at the 7th frame.

4.13.4、Address 03h (Auto Play Setting Register 2)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value		
name	_			T1							

T1 is used to set the frame duration.

When T1=0, FDT=11ms ×64.

When T1= $1\sim63$, FDT=11ms×T1.

The value range of T1 is $0\sim63$, the coefficient of 11ms is typical, and the actual deviation is 20%.

4.13.5, Address 04h(NC)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name				N	C				0x00

Reserved bit

Read and write, but setting any value has no effect.

4.13.6 Address 05h (display setting register)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name	_	_	PS		BE		T2		0x00

PS= 0 Each frame uses the configuration in the corresponding frame data

register.

PS= 1 All frames use the configuration in the data register of frame 1 uniformly.

BE= 0 Do not use the blinking function.

BE= 1 You can use the blinking function.

T2 is used to set the blinking period.

BPT= $0.27s \times T2$

The value range of T2 is $0\sim7$, the coefficient of 0.27s is typical, and the actual deviation is 20%.

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4.13.7, Address 06h (audio synchronization setting register)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name								VE	0x00

VE= 0 Music synchronization mode is off.

VE= 1 The audio signal can control the brightness of the whole lattice.

When VE is set to 1, the input audio signal can affect the current output to the LED, and the brightness of the lattice is controlled by the input audio signal and the data of the PWM register of each LED.

4.13.8. Address 07h (frame number register) (read-only)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name		_		END	_		CN		0x00
		` •		eared when	<i>O</i> ,				
END=	0	Indicates that the picture playback is not finished in the automatic playback mode.							
END=	1	Indicates mode.	that the p	picture play	back ends	in the a	utomatic	playback	

CN=	000	Indicates that the first frame graph is currently displayed.
CN=	001	Indicates that the second frame graph is currently displayed.
CN=	010	Indicates that the third frame graph is currently displayed.
CN=	011	Indicates that the fourth frame graph is currently displayed.
CN=	100	Indicates that the fifth frame graph is currently displayed.
CN=	101	Indicates that the currently displayed figure is frame 6.
CN=	110	Indicates that the currently displayed figure is the seventh frame.
CN=	111	Indicates that the eighth frame graph is currently displayed.

4.13.9 Address 08h (respiratory effect control register 1)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name	_		T3		_		T4		0x00

T3 is used to set the fade-out time.

 $FOT=26ms \times 2^{T3}$

The value range of T3 is $0\sim7$, the coefficient of 26ms is typical, and the actual deviation is 20%.

T4 is used to set the fade-in time.

 $FIT=26ms \times 2^{T4}$

The value range of T4 is $0\sim7$, the coefficient of 26ms is typical, and the actual deviation is 20%.

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4.13.10. Address 09h (respiratory effect control register 2)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name				BE			T5		0x00

BE= 0 In picture mode and auto play mode, breathing light function is turned

off.

BE= 1 In picture mode and auto play mode, breathing light function is turned

on.

T5 is used to set the extinguishing state holding time (ET=Extinguish Time). ET=3.5ms $\times 2$ ^{T5}

The value range of T5 is $0\sim7$, the coefficient of 3.5ms is a typical value, and the actual deviation is 20%.

4.13.11, Address 0Ah (software shutdown control register)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name			_	_			SS	SD	0x00

SSD= 00 In mode 1, the frame data register and the function register can be

written.

SSD= 01 Normal working mode

4.13.12, Address 0Bh (audio control register 1)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name		_		HS	VIE		VG		0x00

HS= 0 Low speed mode

HS= 1 High speed mode

VIE= 0 Music signal input function is turned off.

VIE= 1 Music signal input function is turned on.

VG= 000 The input gain of music signal is 0dB.

VG= 001 Music signal input gain is 3dB.

VG= 010 Music signal input gain 6dB

VG= 011 Music signal input gain 9dB

VG= 100 The music signal input gain is 12dB.

VG= 101 Music signal input gain is 15dB.

VG= 110 Music signal input gain is 18dB.

VG= 111 Music signal input gain is 21dB.



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4.13.13 Address 0Ch AUDIO (audio control register 2)

place	D7	D6	D5	D4	D3	D2	D1	D0	Reset value
name				Т	6				0x00

(Effective in Music Synchronization Mode)

T6 is used to set the music signal input sampling rate (AAR=Audio ADC Rate).

When T6=0, AAR= $\tau \times 256$.

When T6= $1\sim255$, AAR= $46us\times T6$.

The value range of T6 is $0\sim255$, the coefficient of 46us is typical, and the actual deviation is 20%.

4.14 \ Function Description

4.14.1, Current Setting

The average output current of AiP3331 for each LED is controlled by external resistance (resistance R _{EXT} from REXT port to ground), and the output current can be calculated by the following methods:

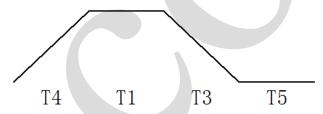
$$I_{LED}\!\!=\!\!64.7/R_{EXT}$$

Example: R _{EXT}= $10K\Omega$, then I _{LED}=6.47ma.

It is recommended that the R $_{EXT}$ resistance be set in the range of $18K\Omega{\sim}25K\Omega$, and the minimum value is $10K\Omega$.

4.14.2 Breathing Light Mode Settings

AiP3331 has built-in automatic breathing light effect, which can control the whole process of breathing effect by setting the time of T1, T3, T4 and T5 in the instruction.



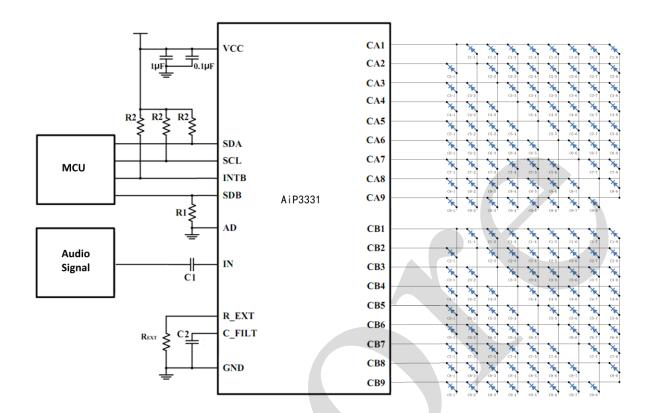
4.14.3 Matters Needing Attention

AiP3331 can drive up to 144 LEDs, but if it is not necessary to use all the positions, the switch control bits corresponding to the unused LED positions must be written with 0 (that is, the software sets the unused position to OFF). Otherwise, other normally connected LEDs will be dimmed.



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5. Typical Application Circuit

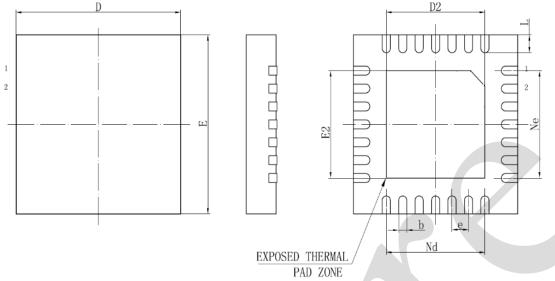


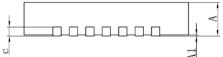


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6. Package Information

6.1、QFN28





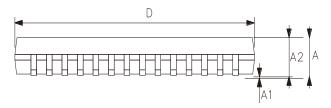
BOTTOM VIEW

2024/01/B	Dimensions	In Millimeters		
Symbol	Min	Max		
A	0.70	0.80		
A1	0	0.05		
b	0.15	0.25		
С	0.18	0.25		
D	3.90	4.10		
Е	3.90	4.10		
D2	2.30	2.70		
E2	2.30	2.70		
e	(0.40		
Nd	2.40			
Ne	2.40			
L	0.35	0.45		

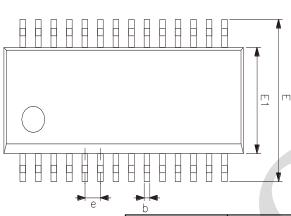


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6.2, SSOP28





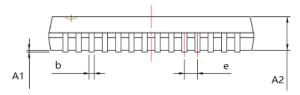


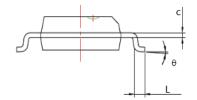
2023/12/A	Dimensions I	n Millimeters		
Symbol	Min	Max		
A		1.75		
A 1	0.02	0.25		
A2	1.30	1.60		
b	0.23	0.31		
c	0.19	0.25		
D	9.75	10.00		
E	5.80	6.45		
E1	3.75	4.00		
e	0.6	35		
L	0.35	0.80		
θ	0 °	8°		

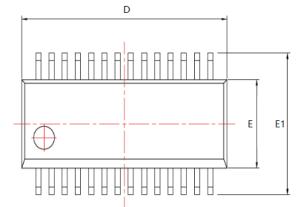


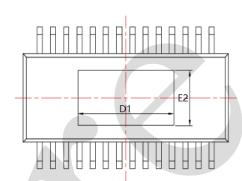
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6.3, ESSOP28









2023/12/A	Dimensions I	n Millimeters
Symbol	Min	Max
A1	0.02	0.08
A2	1.40	1.50
b	0.2	54
С	0.2	03
D	9.75	9.85
D1	4.6	50
Е	3.75	3.85
E2	2.5	50
E1	6.25	6.45
e	0.6	35
L	0.35	0.65
θ	0 °	8°

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7. Statements And Notes

7.1. The name and content of Hazardous substances or Elements in the product

	Hazardous substances or Elements									
Part name	Lead and lead compo unds	Mercur y and mercur y compo unds	Cadm ium and cadmi um comp ounds	Hexaval ent chromiu m compoun ds	Polybro minated biphenyl s	Polybro minate d biphen yl ethers	Dibutyl phthala te	Butylbe nzyl phthala te	Di-2-et hylhex yl phthala te	Diisobu tyl phthala te
Lead frame	0	0	0	0	0	0	0	0	0	0
Plastic resin	0	0	0	0	0	0	0	0	0	0
Chip	0	0	0	0	0	0	0	0	0	0
The lead	0	0	0	0	0	0	0	0	0	O
Plastic sheet installed	0	0	0	0	0	0	0	0	0	0
explanation	 i. Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. i. Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements. 									

7.2. Notes

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