AiP33622
2-Line Serial Interface/Common Cathode 13Seg×7Grid LED Driver and Controller with Constant Current

Product Specification

Specification Revision History：

Version	Date	Description
2023-11-A0	2023-11	New
2024-09-A1	2024-09	Modify parameters

Contents

1、General Description

AiP33622 is a dot matrix LED driver controller that can drive common cathode LED dot matrices in constant current mode. The circuit provides 7 GRIDs and 13 SEGs, which can drive various size LED panels according to needs. The circuit can adjust the brightness of a single point to 256 levels of PWM.

AiP33622 is equipped with IIC communication interface, constant current control module, display data RAM, oscillator and other modules. It can be directly connected to the master device to achieve display control with the minimum peripherals.

AiP33622 provides more display functions and its instruction set is compatible with traditional constant voltage LED products such as AiP1628 and AiP1640, making it convenient for software engineers to quickly transplant programs and shorten the development cycle of the solution.

Features:

- Driving matrix size: Maximum 7 GRID×13 SEG, common cathode LED dot matrix, GRID number selectable
- Global brightness adjustment:
  Software can adjust the global constant current size, with 64-step constant current control
- Single point brightness adjustment
  Each point supports 256-level PWM brightness adjustment
- Built-in display data memory (DDRAM)
- Communication interface: IIC interface
- Built-in clock module
- Built-in power on reset circuit
- Built-in sleep mode for low power standby
- Built-in blanking circuit
- Supply voltage: 2.7V to 5.5V
- Packaging information: QFN24/SOP24/ESSOP24

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP33622QB24.TB	QFN24	AiP33622	490 PCS/plate	10 plate/box	4900 PCS/box	Dimensions of plastic enclosure: 4.0mm×4.0mm Pin spacing: 0.5mm

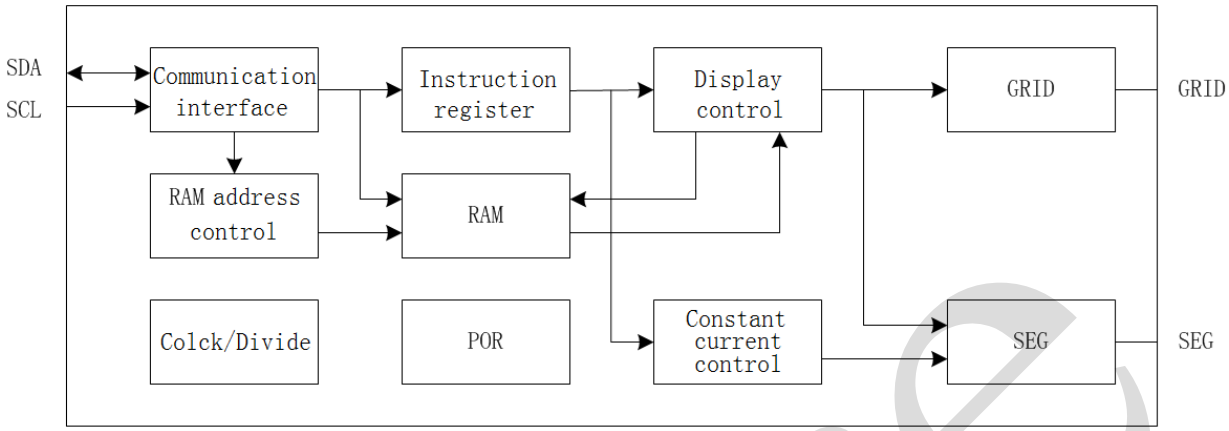
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP33622SA24.TR	SOP24	AiP33622	1250PCS/reel	1250PCS/box	Dimensions of plastic enclosure: 15.4mm×7.5mm Pin spacing: 1.27mm
AiP33622VE24.TR	ESSOP24	AiP33622	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 8.6mm×3.9mm Pin spacing: 0.635mm
AiP33622QB24.TR	QFN24	AiP33622	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 4.0mm×4.0mm Pin spacing: 0.5mm

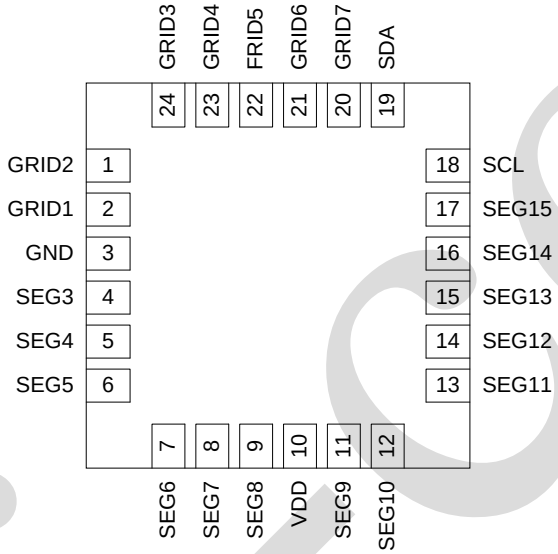
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

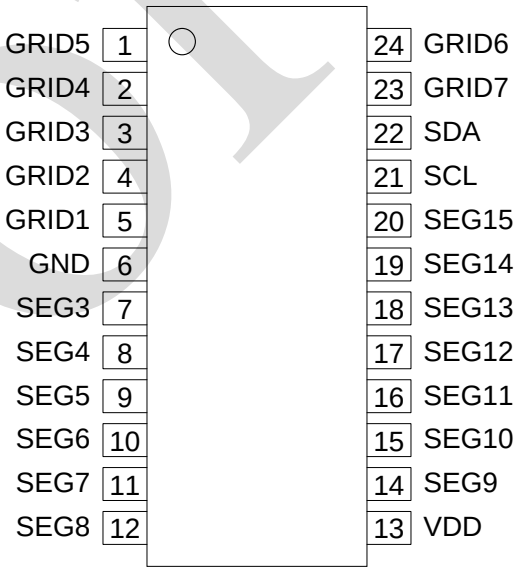
2.1、Block Diagram



2.2、Pin Configurations



QFN24



SOP24/ESSOP24

2.3、Pin Description

Pin Name	IO	Description
VDD	P	power supply
GND	P	ground
SCL	I	communication interface clock input
SDA	IO	communication interface data
GRID1~7	O	LED driver common, cathode drive
SEG3~15	O	LED driver constant current terminal, anode drive

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, unless otherwise specified)

Characteristic	Symbol	Conditions	Value	Unit
power supply voltage	VDD	-	-0.3 to +6.0	V
input voltage	VIN	-	-0.3 to VDD+0.3	V
operating temperature	T_{amb}	-	-40 to +85	℃
storage temperature	T_{stg}	-	-65 to +150	℃
soldering temperature	T_L	10s	260	℃

3.2、Electrical Characteristics

3.2.1、DC Characteristics

(T_{amb}=25℃, VDD=5V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	VDD	-	2.7	-	5.5	V
HIGH-level input voltage	VIH	VDD=5V, SCL, SDA	3.0	-	VDD	V
LOW-level input voltage	VIL	VDD=5V SCL, SDA	0	-	1.5	V
HIGH-level output current	IOH	VDD=5V, SEG Software I[4:0]=11111 SEG voltage 4V	-	30	-	mA
LOW-level output current	IOL	VDD=5V, GRID GRID voltage 0.4V	500	-	-	mA
supply current	IDD	VDD=5V display OFF, no load	-	-	5	mA
sleep current	ISLEEP	VDD=5V display OFF, sleep mode	-	-	300	uA

VDD can ensure normal operation of the logic part within the range of 2.7V to 4.0V, but the output constant current will be affected by a low power supply voltage, and cannot output in the theoretical state. The minimum power supply requirement for VDD in different peripheral LED conditions is as follows:
Minimum operating voltage for red LED: 4.0V
Minimum operating voltage for yellow LED: 4.0V
Minimum operating voltage for green LED: 5.0V
Minimum operating voltage for blue LED: 5.0V
Minimum operating voltage for white LED: 4.5V
Minimum operating voltage for RGB mode LED controlled by AiP33622: 5.0V

If the working voltage conditions are not met, the output current will be lower than the set value, affecting brightness. This problem is caused by the intrinsic properties of the LED, and is unrelated to the number of LEDs lit simultaneously or the performance of the driver.

3.2.2、AC Characteristics

(T_{amb}=25℃, VDD=5V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
serial communication frequency	f_{SCL}	-	-	-	1	MHz
bus idle time	t_{BUF}	-	-	0.5	-	us
Start condition hold time	$t_{HD,STA}$	-	-	0.26	-	us
setup time for restart state	$t_{SU,STA}$	-	-	0.26	-	us
Stop condition setup time	$t_{SU,STO}$	-	-	0.26	-	us
data hold time	$t_{HD,DAT}$	-	-	0	-	us
data setup time	$t_{SU,DAT}$	-	-	50	-	ns
SCL low level time	t_{LOW}	-	-	0.5	-	us
SCL high level time	t_{HIGH}	-	-	0.26	-	us
rise time for SDA, SCL	t_R	-	-	-	300	ns
fall time for SDA, SCL	t_F	-	-	-	300	ns

4、Function Description

4.1、Serial Interface

AiP33622 provides a IIC communication interface with the following features:

● SCL、SDA two-wire communication (SDA is an NMOS open-drain output with an internal 5KΩ pull-up resistor)

● require start and stop conditions to identify restart operations

● slave address required

● handshake signal ACK bit is required

● 9 clocks per cycle, high bit first

4.1.1、Start and Stop Conditions

AiP33622 detects the start and stop conditions when the clock signal is HIGH.

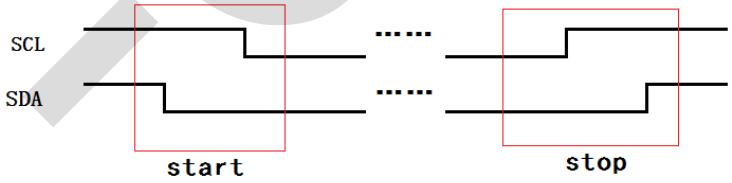


Figure 1 Start and stop conditions waveforms

Therefore, data can only be changed during the low-voltage clock period, otherwise incorrect start (restart) and stop conditions will appear.

4.1.2、Slave Address

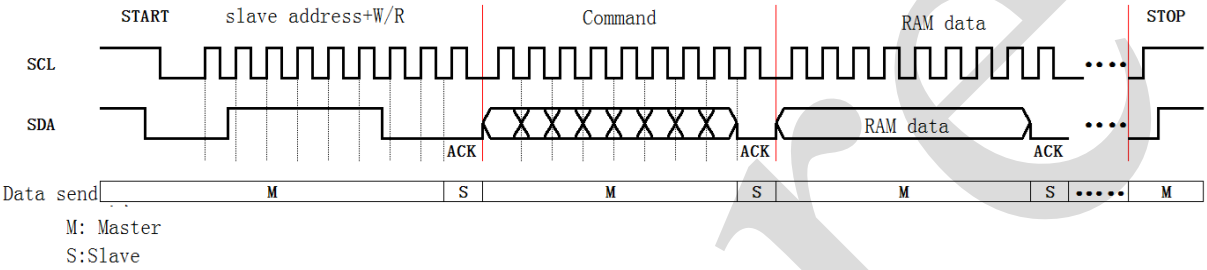
The slave address of AiP33622:

B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	1	1	0	0	W/R

The lowest B0 is the read/write bit. When W/R=0, subsequent write operations are performed. Do not read.

4.1.3、Communication Format

Write data process:



Communication process:

1. The master sends the START (or restart) signal
2. The master sends the slave address and the W/R control bit (set to 0 when writing data), and the slave feeds back ACK.
3. The master sends the command, and the slave feeds back ACK.
4. The master sends the RAM data, and the slave feeds back ACK.
5. At the end, the master sends the STOP signal.

The first byte after the START (or reSTART) signal is identified to the slave address and the W/R control bit. When the input slave address matches the circuit, the circuit feeds back ACK and can continue subsequent communication; when the slave address does not match, the circuit feeds back NAK and ignores all subsequent data.

The second byte of the communication is identified as the command, AiP33622 cannot write commands continuously. If need to configure the second command, must stop the communication and start again, or directly use reSTART to restart. However, it must be noted that the current communication cycle can be ended only after the 9th clock input (that is, the ACK) process is completed, otherwise the commands entered by the first 8 clocks are invalid.

When W/R=0, the third byte of communication starts to STOP, and all written data is recognized as display data and written to the built-in RAM. The RAM data here determines the address of the RAM to be written according to the state of the ADS bits in the command.

When ADS=0, the data must be written from the address 0x00, and the RAM address is automatically increased by 1 for each byte entered.

When ADS=1, the starting address of the RAM is controlled by the ADDR bit in the instruction, and the RAM address automatically increments by 1 for each input byte.

Between a set of start/stop, the number of effective bytes of input RAM data is controlled by the G_N bit, and when the number of consecutive bytes written exceeds the maximum number of bytes determined by

the G_N bit, the excess data is ignored:

G_N setting value	Number of scan lines	RAM address range (ADS=0)	RAM address range (ADS=1)
0	1line, GRID1 valid	0x00~0x0F	ADDR~0x0F
1	2 lines, GRID1~2 valid	0x00~0x1F	ADDR~0x1F
2	3 lines, GRID1~3 valid	0x00~0x2F	ADDR~0x2F
3	4 lines, GRID1~4 valid	0x00~0x3F	ADDR~0x3F
4	5 lines, GRID1~5 valid	0x00~0x4F	ADDR~0x4F
5	6 lines, GRID1~6 valid	0x00~0x5F	ADDR~0x5F
6	7 lines, GRID1~7 valid	0x00~0x6F	ADDR~0x6F

When writing data exceeds the RAM address range, the circuit feeds back NAK.

*Note: Do not set the value to 7 to 15.

4.2、Command System

Command	Command data								Note
1	0	0	I5	I4	I3	I2	I1	I0	Constant current setting
2	0	1	0	0	G_N3	G_N2	G_N1	G_N0	Number of GRID scan lines
3	0	1	0	1	DT1	DT0	TP2	TP1	DT: GRID dead time TP: temperature protection selection
4	0	1	1	0	SVGD	ADS	0	SLEEP	SVGD: output impedance regulation ADS: RAM partial rewrite SLEEP: sleep mode
5	1	0	0	0	FR1	FR0	DON	GS	FR: frame frequency DON: on/off display GS: on/off SEG blanking
6	1	0	0	1	0	0	GRE	LVRE	GRE: global reset LVRE: enable LVR
7	1	1	0	0	AD7	AD6	AD5	AD4	RAM address high bit
8	1	1	1	0	AD3	AD2	AD1	AD0	RAM address low bit

Command	Command data								Note
1	0	0	I5	I4	I3	I2	I1	I0	Constant current setting
I[5:0]	Reset value: I[5:0]=000000 SEG output current=0.375mA ×(17+I[5:0]) 000000: minimum current is 6.375mA 111111: maximum current is 30mA								

Command	Command data								Note
2	0	1	0	0	G_N3	G_N2	G_N1	G_N0	Number of GRID scan lines
G_N[3:0]	Reset value: G_N[3:0]=0111 G_N[3:0]=0, scan 1 lines, only GRID1 valid G_N[3:0]=1, scan 2 lines, only GRID1~2 valid G_N[3:0]=2, scan 3 lines, only GRID1~3 valid G_N[3:0]=3, scan 4 lines, only GRID1~4 valid G_N[3:0]=4, scan 5 lines, only GRID1~5 valid G_N[3:0]=5, scan 6 lines, only GRID1~6 valid G_N[3:0]=6, scan 7 lines, only GRID1~7 valid G_N[3:0]=7~15, do not use								

Command	Command data								Note
3	0	1	0	1	DT1	DT0	TP2	TP1	DT: GRID dead time TP: temperature protection selection
DT[1:0]	Reset value: DT[1:0]=00 DT[1:0]=00, GRID dead time is 4 system clocks (about 0.5us) DT[1:0]=01, GRID dead time is 8 system clocks DT[1:0]=10, GRID dead time is 16 system clocks DT[1:0]=11, GRID dead time is 24 system clocks								
TP2	Reset value: TP2=0 TP2=0, when the IC temperature is higher than 150℃, SEG is off. TP2=1, this temperature protection is not used.								
TP1	Reset value: TP1=0 TP1=0, when the IC temperature is higher than 125℃, SEG output current is reduced to 2/3 of the setting value. TP1=1, this temperature protection is not used.								

Command	Command data								Note
4	0	1	1	0	SVGD	ADS	0	SLEEP	SVGD: output impedance regulation ADS：RAM address added automatically SLEEP: sleep mode
SVGD	Reset value: SVGD=0 SVGD=0: recommended setting to 0 when SEG output current<10mA SVGD=1: recommended setting to 1 when SEG output current≥10mA								
ADS	Reset value: ADS=0 ADS=0, when RAM reads and writes, the address is automatically added from 0x00 ADS=1, when RAM reads and writes, the address is automatically added from AD[7:0]								
SLEEP	Reset value: SLEEP=0 SLEEP=1, turn off the analog module and the display command together to enter the sleep state Sleep state: GRID: the current GRID remains in output and the other GRIDs are off SEG: all off, high-impedance state Clock: off Reference: working Current amplification: off								

Command	Command data								Note
5	1	0	0	0	FR1	FR0	DON	GS	FR: frame frequency DON: on/off display GS: on/off SEG blanking
FR[1:0]	Reset value: FR[1:0]=00 FR[1:0]=00, set 7 line scan, frame frequency is about 500Hz FR[1:0]=01, set 7 line scan, frame frequency is about 1000Hz FR[1:0]=10, set 7 line scan, frame frequency is about 2000Hz FR[1:0]=11, set 7 line scan, frame frequency is about 4000Hz								
DON	Reset value: DON=0 DON=0, display off DON=1, display on								
GS	Reset value: GS=0 GS=0, disable SEG blanking function GS=1, enable SEG blanking function								

Command	Command data								Note
6	1	0	0	1	0	0	GRE	LVRE	GRE: global reset LVRE: enable LVR
GRE	Reset value: GRE=0 GRE=1 perform software reset, this bit is automatically cleared after stop condition software reset All command registers restore reset values The data in RAM is unchanged								
LVRE	Reset value: LVRE=0 LVRE=0, disable power-off reset function LVRE=1, enable power-off reset function, LVR voltage is about 2V								

Command	Command data								Note
7	1	1	0	0	AD7	AD6	AD5	AD4	RAM address high bit
8	1	1	1	0	AD3	AD2	AD1	AD0	RAM address low bit
AD[7:0]	Reset value: AD[7:0]=0000 0000 When ADS=1, this bit controls the RAM start address. When ADS=0, can set the bit, but it has no effect.								

4.3、RAM

RAM has 144 addresses with 8 bit data for each address. The data of each address is used to control the SEG output valid time of one LED.

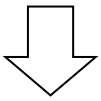
The corresponding relationship between RAM address and LED dot matrix is as follows:

AD[7:4] / AD[3:0]	0000	0001	0010	0011	0100	0101	0110	0111	1000*
0000	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid
0001	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid
0010	G1S3	G2S3	G3S3	G4S3	G5S3	G6S3	G7S3	invalid	invalid
0011	G1S4	G2S4	G3S4	G4S4	G5S4	G6S4	G7S4	invalid	invalid
0100	G1S5	G2S5	G3S5	G4S5	G5S5	G6S5	G7S5	invalid	invalid
0101	G1S6	G2S6	G3S6	G4S6	G5S6	G6S6	G7S6	invalid	invalid
0110	G1S7	G2S7	G3S7	G4S7	G5S7	G6S7	G7S7	invalid	invalid
0111	G1S8	G2S8	G3S8	G4S8	G5S8	G6S8	G7S8	invalid	invalid
1000	G1S9	G2S9	G3S9	G4S9	G5S9	G6S9	G7S9	invalid	invalid
1001	G1S10	G2S10	G3S10	G4S10	G5S10	G6S10	G7S10	invalid	invalid
1010	G1S11	G2S11	G3S11	G4S11	G5S11	G6S11	G7S11	invalid	invalid
1011	G1S12	G2S12	G3S12	G4S12	G5S12	G6S12	G7S12	invalid	invalid
1100	G1S13	G2S13	G3S13	G4S13	G5S13	G6S13	G7S13	invalid	invalid
1101	G1S14	G2S14	G3S14	G4S14	G5S14	G6S14	G7S14	invalid	invalid
1110	G1S15	G2S15	G3S15	G4S15	G5S15	G6S15	G7S15	invalid	invalid
1111	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid

Note: GnSn stands for cathode connected to GRIDn, anode connected to SEGn LED.

*** Note: Physical space for "invalid" bits actually exists, but there is no corresponding port, so data can be written to these addresses, but it has no effect.**

The corresponding relationship between the data in RAM and the duty cycle of LED lighting time:

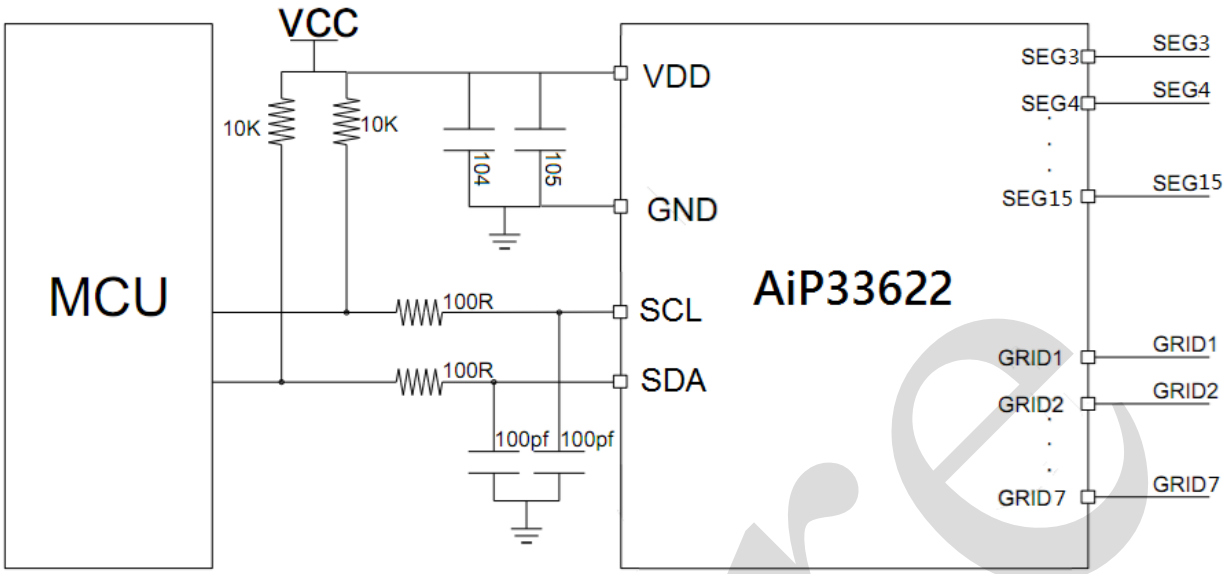
Data in RAM	Corresponding LED Lighting Time
0x00	Not bright (SEG off)
0x01	
……	
0xFE	
0xFF	Brightest (SEG takes the longest time to open)

RAM address range self-addition will change with different G_N settings.

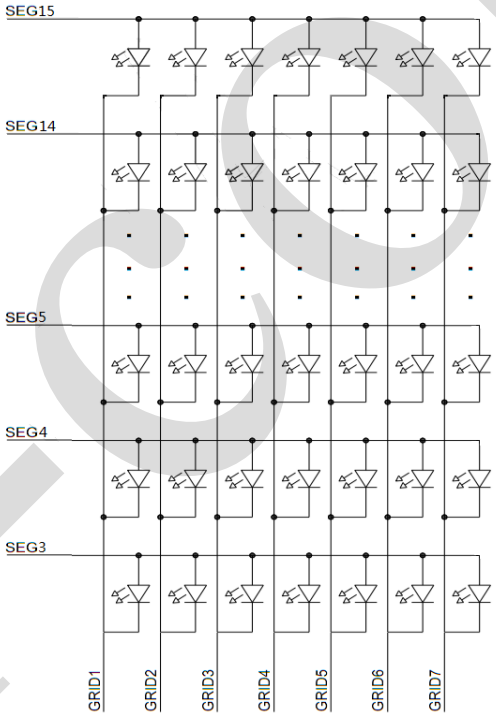
G_N setting value	Number of scan lines	RAM address range (AD=0)	RAM address range (AD=1)
0	1 line, GRID1 valid	0x00~0x0F	ADDR~0x0F
1	2 lines, GRID1~2 valid	0x00~0x1F	ADDR~0x1F
2	3 lines, GRID1~3 valid	0x00~0x2F	ADDR~0x2F
3	4 lines, GRID1~4 valid	0x00~0x3F	ADDR~0x3F
4	5 lines, GRID1~5 valid	0x00~0x4F	ADDR~0x4F
5	6 lines, GRID1~6 valid	0x00~0x5F	ADDR~0x5F
6	7 lines, GRID1~7 valid	0x00~0x6F	ADDR~0x6F

*Note: Do not set the value to 7 to 15.

5、Typical Application Circuit

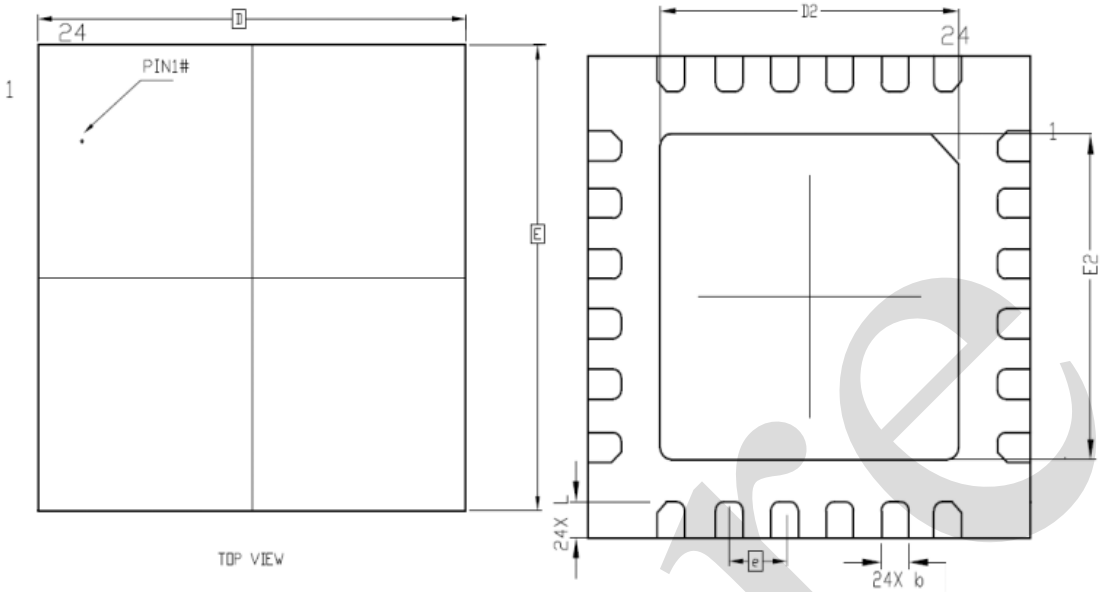


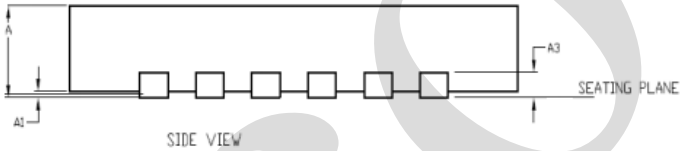
Note: Determine whether to add the ground capacitance of the SDA and SCL ports as required.



6、Package Information

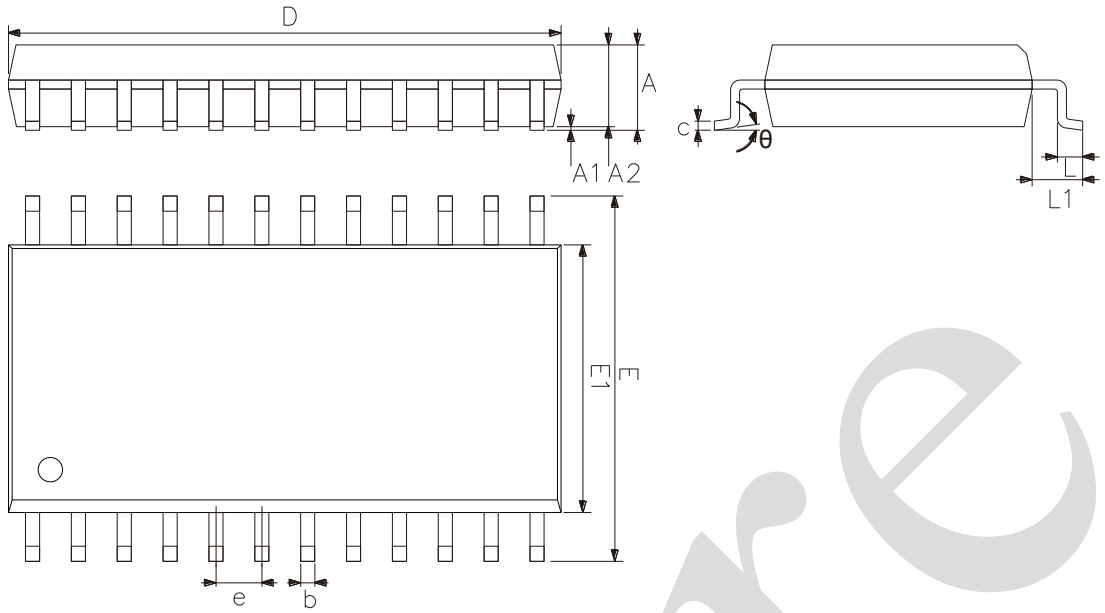
6.1、QFN24





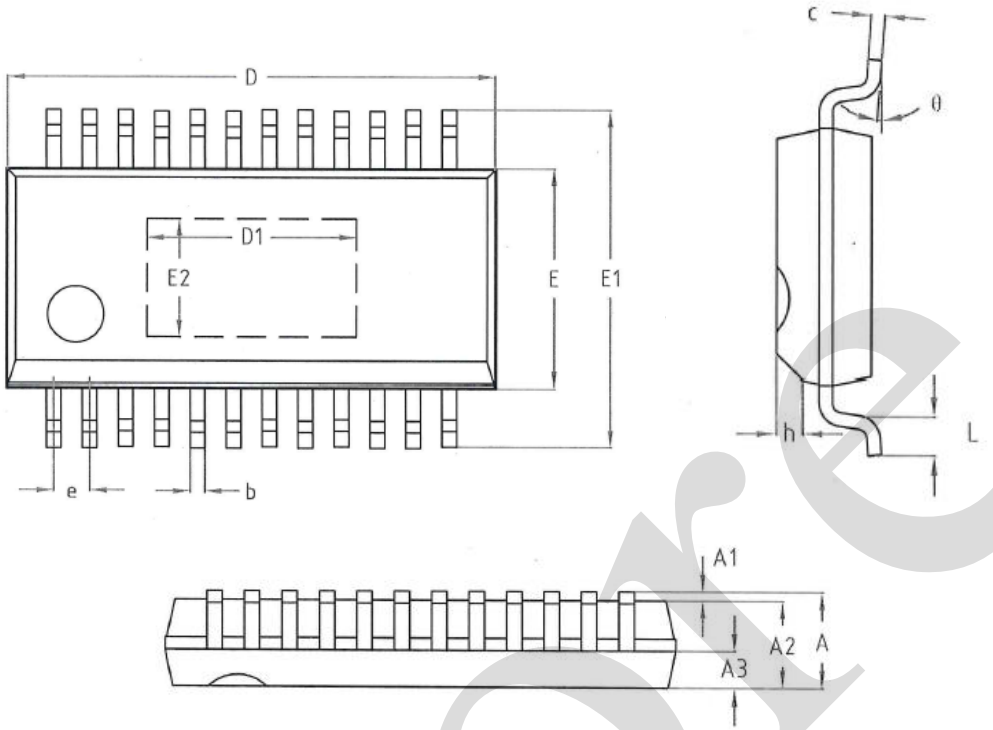
2024/01/B	Dimensions In Millimeters	
Symbol	Min	Max
A	0.70	0.80
A1	0	0.05
A3	0.20	
b	0.20	0.30
D	3.90	4.10
E	3.90	4.10
D2	2.60	2.80
E2	2.60	2.80
e	0.50	
L	0.25	0.45

6.2、SOP24



2023/12/A	Dimensions In Millimeters	
Symbol	**Min.**	**Max.**
A	2.35	2.65
A1	0.10	0.30
A2	2.13	2.44
b	0.39	0.47
c	0.25	0.30
D	15.19	15.55
E	10.10	10.57
E1	7.40	7.62
e	1.27	
L	0.41	1.00
L1	1.30	1.50
θ	0°	8°

6.3、ESSOP24



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	—	1.75
A1	0.10	0.25
A2	1.35	1.55
A3	0.60	0.70
b	0.23	0.31
c	0.19	0.25
D	8.50	8.70
D1	3.70	
E	3.80	4.00
E1	5.80	6.20
E2	2.10	
e	0.635	
h	0.30	0.50
L	0.40	0.80
θ	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

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