AiP24C256
I2C Serial EEPROM

Product Specification

Specification Revision History ：

Version	Data	Description
2022-08-A1	2022-08	New-made
2023-02-B1	2023-02	Update the template
2024-04-B2	2024-04	Modify the content

Contents

1、General Description

AiP24C256 is a 256-Kbit serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 32768 × 8bits, which is organized in 64-byte per page. The device features I^2C interface, it is used in low-voltage and low-power systems.

Features:

- Write protection pin provides hardware data protection
- Wide Operating voltage range 1.8V to 5.5V
- Internal structure of memory: 32768×8(256K)
- 2-line serial interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional data propagation protocols
- Clock range: 400 kHz(1.8V to 2.5V) and 1MHz(2.5V to 5.5V)
- 64 byte Page Write Modes
- Partial Page Writes Allowed
- Additional write lock page
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - Endurance: >2 Million Write Cycles
  - Data Retention: >100 Years
- Package: DIP8, SOP8, TSSOP8

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP24C256DA8.TB	DIP8	AiP24C256	50 PCS/tube	40 tube/box	2000 PCS/box	Dimensions of plastic enclosure: 9.2mm×6.4mm Pin spacing: 2.54mm
AiP24C256SA8.TB	SOP8	AiP24C256	100 PCS/tube	100 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
AiP24C256TB8.TB	TSSOP8	24C256	100 PCS/tube	200 tube/box	20000 PCS/box	Dimensions of plastic enclosure: 4.4mm×3.0mm Pin spacing: 0.65mm

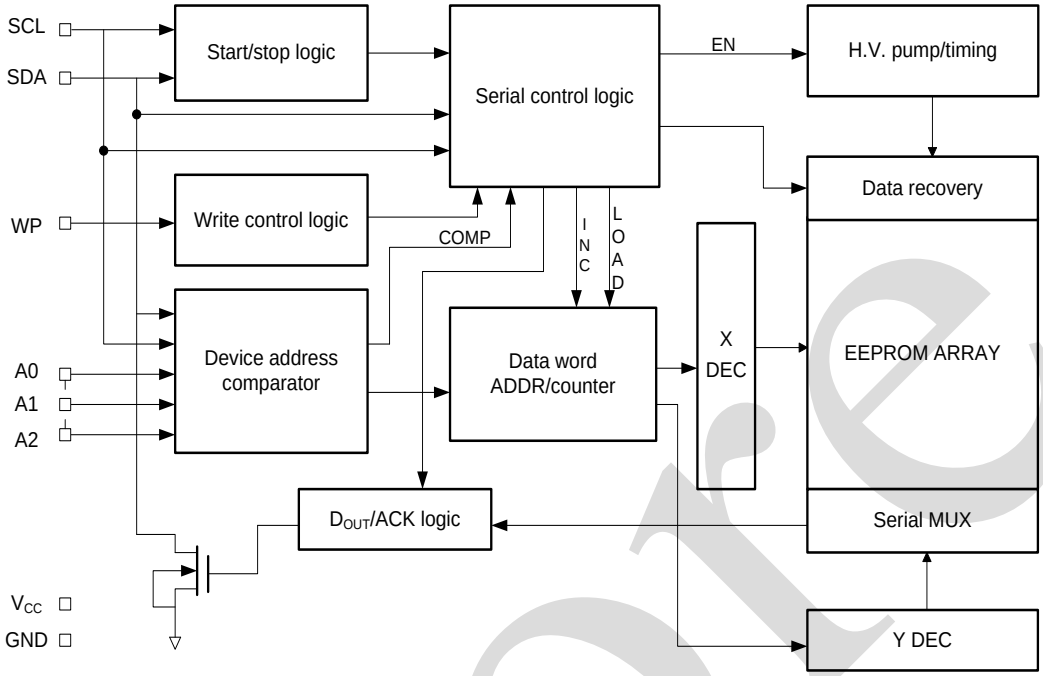
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP24C256SA8.TR	SOP8	AiP24C256	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing:1.27mm
AiP24C256TB8.TR	TSSOP8	24C256	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 4.4mm×3.0mm Pin spacing:0.65mm

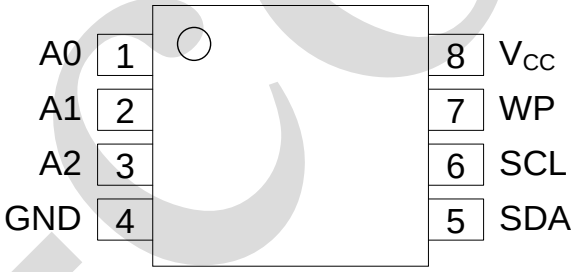
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	A0	Device Address Input: Pins A2, A1 and A0 are device address inputs. Generally, pins A2, A1 and A0 are used for hardware addressing, and a total of 8 devices can be connected on a single bus system. If these pins are left floating, pins A2, A1 and A0 will be pulled down to GND internally.
2	A1	
3	A2	
4	GND	Ground
5	SDA	Serial Data: SDA pin is a bidirectional port for data propagation. This pin is open-drain driven and can be wired or logically operated with any number of other open-drain or open-collector devices.
6	SCL	Serial Clock: Data is sent into EEPROM on the rising edge of SCL clock; and data is sent from EEPROM On the falling edge of SCL clock.
7	WP	Write Control The WP pin can provide hardware data protection. Normal read/write operation is allowed when WP pin is connected to ground. Write protection is performed when WP is connected to VCC.
8	Vcc	Power

Conditions of Write Protection	Parts of Write Protection
V_{CC}	All (256K)
GND	Normal read/write operation

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Conditions		Value	Unit
Power Supply Voltage	Vcc	-		6.25	V
Voltage on Any Pin with Respect to Ground	V	-		-1.0 to +7.0	V
DC Output Current	I	-		5.0	mA
Input/Output Capacitance (SDA)	$C_{I/O}$	T_{amb}=25℃, f=1.0MHz, V_{CC}=5V, $V_{I/O}$=GND, Note 1		8	pF
Input Capacitance (A0, A1, A2, SCL)	C_{IN}	T_{amb}=25℃, f=1.0MHz, V_{CC}=5V, $V_{I/O}$=GND, Note 1		6	pF
Operating Temperature	T_{amb}	-		-40 to +85	℃
Storage Temperature	T_{stg}	-		-65 to +150	℃
Soldering Temperature	T_L	10s	DIP	250	℃
			SOP/TSSOP	260	

Notes:

[1] This parameter is ensured by characterization not 100% tested

[2]Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2、Electrical Characteristics

3.2.1、 DC Characteristics

(T_{amb}=-40℃ to +85℃, V_{CC}=+1.8V to +5.5V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	-	1.8	-	5.5	V
Standby Current	Isb	Vcc=3.3V, T_{amb}=85℃	-	-	1.0	uA
		Vcc=5.5V, T_{amb}=85℃	-	-	3.0	uA
Supply Current	I_{CC1}	Vcc=5.5V, Read at 400Khz	-	-	1.0	mA
Supply Current	I_{CC2}	Vcc=5.5V,Write at 400Khz	-	-	2.0	mA
Input Leakage Current	I_{LI}	V_{IN}=V_{CC} or GND	-	0.10	1.0	uA
Output Leakage Current	I_{LO}	V_{OUT}=V_{CC} or GND	-	0.05	1.0	uA
Input Low Level(1)	V_{IL}	-	-0.6	-	0.3V_{CC}	V
Input High Level(1)	V_{IH}	-	0.7V_{CC}	-	V_{CC}+0.5	V
Output Low Level	V_{OL1}	I_{OL}=2.1mA, V_{CC}=3.0V	-	-	0.2	V
Output Low Level	V_{OL2}	I_{OL}=1.5mA, V_{CC}=1.8V	-	-	0.4	V

Notes: [1] V_{IL}(min.) and V_{IH}(max.) are ensured by characterization not 100% tested.

3.2.2、AC Characteristics

(Unless otherwise specified, V_{CC}=1.8V to 5.5V, T_{amb}=-40℃ to +85℃, C_L=100pF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Frequency, SCL	f_{SCL}	V_{CC}=1.8V	-	-	400	kHz
		V_{CC}=2.7V	-	-	1000	
		V_{CC}=5.0V	-	-	1000	
Clock Pulse Width Low	t_{LOW}	V_{CC}=1.8V	1.3	-	-	us
		V_{CC}=2.7V	0.4	-	-	
		V_{CC}=5.0V	0.4	-	-	
Clock Pulse Width High	t_{HIGH}	V_{CC}=1.8V	0.6	-	-	us
		V_{CC}=2.7V	0.4	-	-	
		V_{CC}=5.0V	0.4	-	-	
Noise Suppression Time	t_I	V_{CC}=1.8V	-	-	100	ns
		V_{CC}=2.7V	-	-	50	
		V_{CC}=5.0V	-	-	50	
Clock Low to Data Out Valid	t_{AA}	V_{CC}=1.8V	0.05	-	0.9	us
		V_{CC}=2.7V	0.05	-	0.55	
		V_{CC}=5.0V	0.05	-	0.55	
Time the bus must be free before a new transmission can start	t_{BUF}	V_{CC}=1.8V	1.3	-	-	us
		V_{CC}=2.7V	0.5	-	-	
		V_{CC}=5.0V	0.5	-	-	
Start Hold Time	$t_{HD.STA}$	V_{CC}=1.8V	0.6	-	-	us
		V_{CC}=2.7V	0.25	-	-	
		V_{CC}=5.0V	0.25	-	-	
Start Setup Time	$t_{SU.STA}$	V_{CC}=1.8V	0.6	-	-	us

		V_{CC}=2.7V	0.25	-	-	
		V_{CC}=5.0V	0.25	-	-	
Data In Hold Time	$t_{HD.D}$	V_{CC}=1.8V	0	-	-	us
		V_{CC}=2.7V	0	-	-	
		V_{CC}=5.0V	0	-	-	
Data In Setup Time	$t_{SU.D}$	V_{CC}=1.8V	100	-	-	ns
		V_{CC}=2.7V	100	-	-	
		V_{CC}=5.0V	100	-	-	
Inputs Rise Time	t_R	V_{CC}=1.7V	-	-	300	ns
		V_{CC}=2.7V	-	-	300	
		V_{CC}=5.0V	-	-	300	
Inputs Fall Time	t_F	V_{CC}=1.8V	-	-	300	ns
		V_{CC}=2.7V	-	-	300	
		V_{CC}=5.0V	-	-	100	
Stop Setup Time	$t_{SU.STO}$	V_{CC}=1.8V	0.6	-	-	us
		V_{CC}=2.7V	0.25	-	-	
		V_{CC}=5.0V	0.25	-	-	
Data Out Hold Time	t_{DH}	V_{CC}=1.8V	50	-	-	ns
		V_{CC}=2.7V	50	-	-	
		V_{CC}=5.0V	50	-	-	
WP pin Setup Time	$t_{SU.WP}$	V_{CC}=1.8V	1.2	-	-	us
		V_{CC}=2.7V	0.6	-	-	
		V_{CC}=5.0V	0.6	-	-	
WP pin Hold Time	$t_{HD.WP}$	V_{CC}=1.8V	1.2	-	-	us
		V_{CC}=2.7V	0.6	-	-	
		V_{CC}=5.0V	0.6	-	-	
Write Cycle Time	t_{WR}	V_{CC}=1.8V	-	-	5	ms
		V_{CC}=2.7V	-	-	5	
		V_{CC}=5.0V	-	-	5	
Page mode	EDR	V_{CC}=5V T_{amb}=25℃	2000000	—	—	Write cycles
			100 years	—	—	Data retention

Note: This parameter is ensured by characterization and is not 100% tested.

4、Function Description

4.1、Device Operation

4.1.1、Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 3). Data changes during SCL high periods will indicate a start or stop condition as defined below.

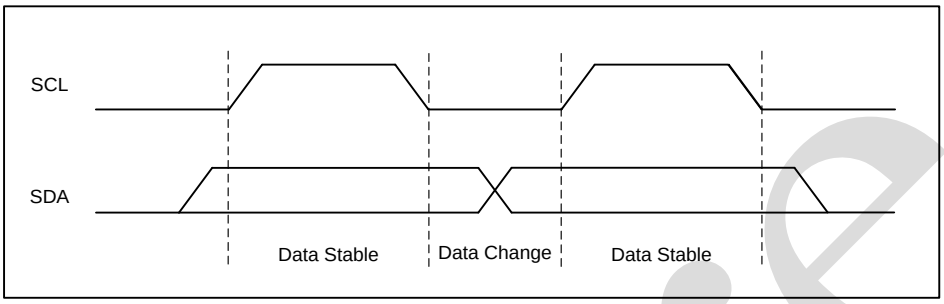


Figure 3

4.1.2、Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 4).

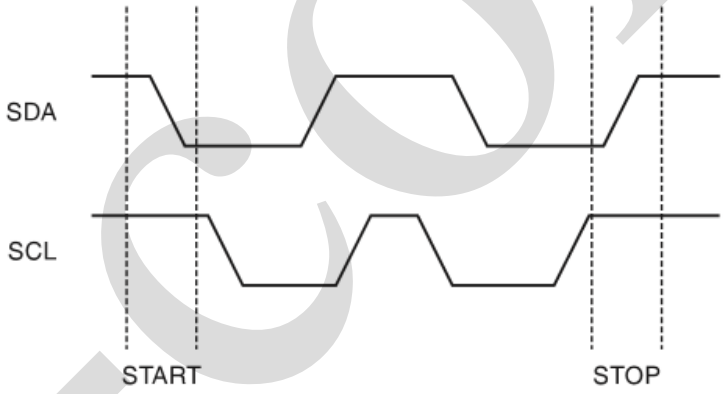


Figure 4

4.1.3、Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition (see Figure 4). After a read sequence, the stop command will place EEPROM in a standby power mode

4.1.4、Acknowledge (ACK)

All addresses and data words are serially transmitted to and from EEPROM in 8-bit words. It sends a low-level signal to acknowledge that it has received each word. This happens during the ninth clock cycle.

4.1.5、Standby Mode

The AiP24C256 features a standby mode which is enabled: (a) after a fresh power up, (b) after completing a self-time internal programming operation.

4.1.6、Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

4.1.7、Bus Timing(see to Figure 5)

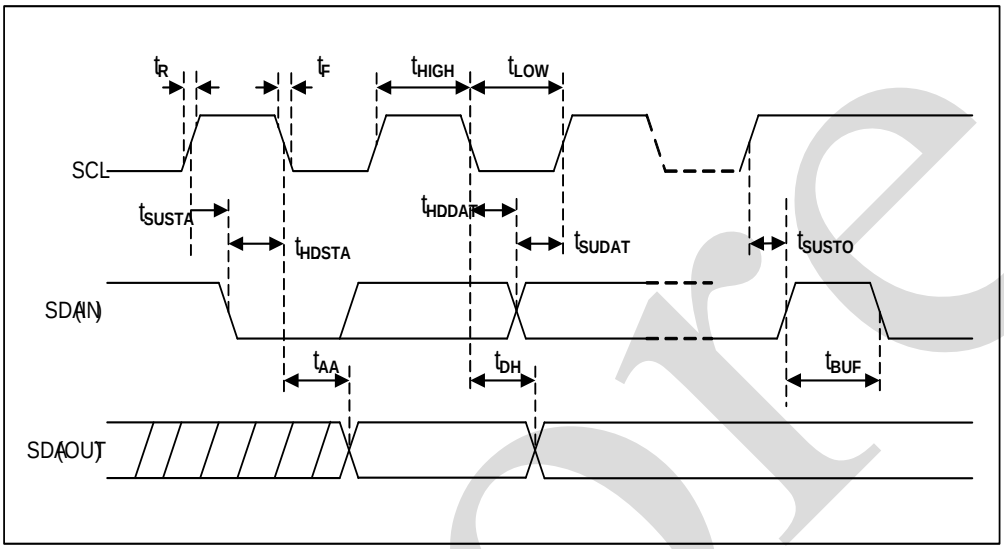
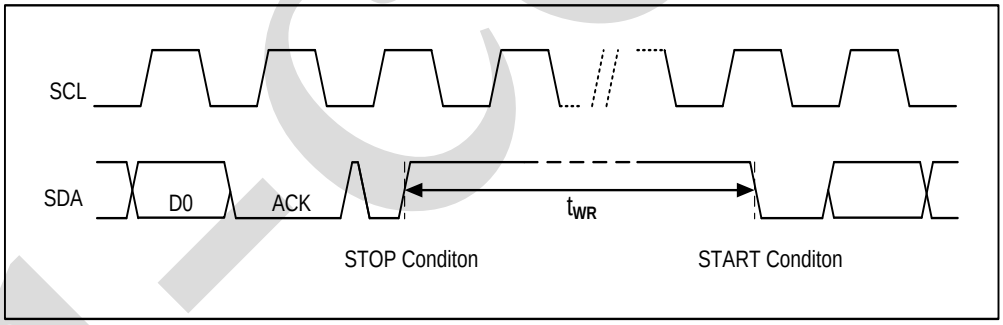


Figure 5

4.1.8、Write Cycle Timing(see to Figure 6)



Note: 1. Write cycle time(t_{wr}) starts from the valid stop status of write sequence and to the end of the internal clear/write cycle.

Figure 6

4.1.9、Output Response(see to Figure 7)

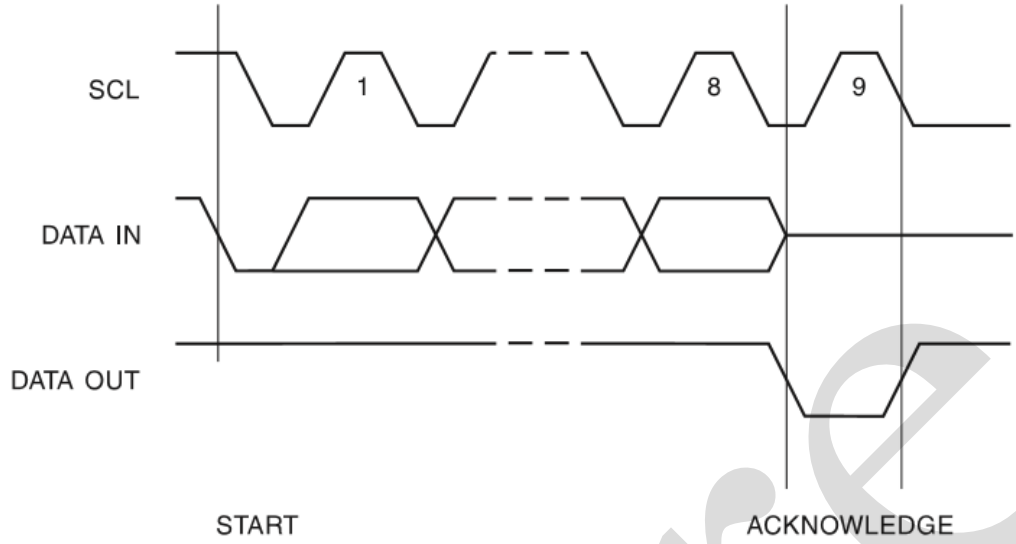


Figure 7

4.2、Device Addressing

The AiP24C64 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table below). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

Table 1 Device Address

MSB							LSB
1	0	1	0	A2	A1	A0	R/W

The first four bits of the device address word are fixed to 1010. The next three bits are A2, A1, and A0 device address bits, they allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, EEPROM will output a low-level signal. If a compare is not made, the device will return to a standby state(see table 2 and table 3).

Table 2 First Word Address

	MSB						
X	B14	B13	B12	B11	B10	B9	B8

Table 3 Second Word Address

							LSB
B7	B6	B5	B4	B3	B2	B1	B0

4.3、Write Operations

4.3.1、Byte Write

The initialization of write operation requires device address, acknowledgment signal and two 8-bit data word addresses. Upon receipt of this address, EEPROM will respond with a low-level response again and then clock read the first 8-bit data word. After the receipt is finished, EEPROM will output a low-level response. The addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then EEPROM enters an internally timed write cycle(t_{wr}), all inputs are disabled during this write cycle and EEPROM will not respond until the write is complete (see Figure 8).

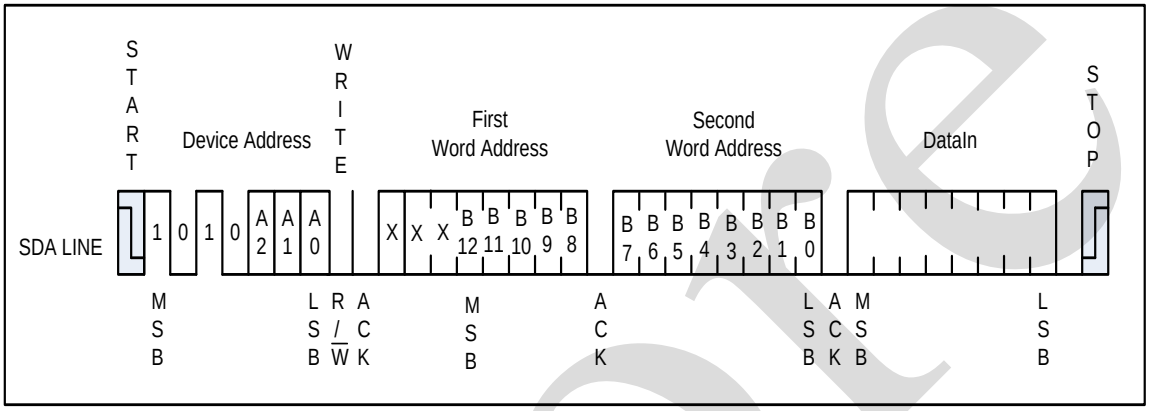


Figure 8

4.3.2、Page Write

The EEPROM of AiP24C256 is 64-byte page write. The initialization process of a page write is as same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, it will propagate the rest 63 bytes after the EEPROM receives 8-bit data and send one response. The EEPROM will send one low-level response after each data word is received. The microcontroller must terminate the page write sequence with a stop condition. (see Figure 9).

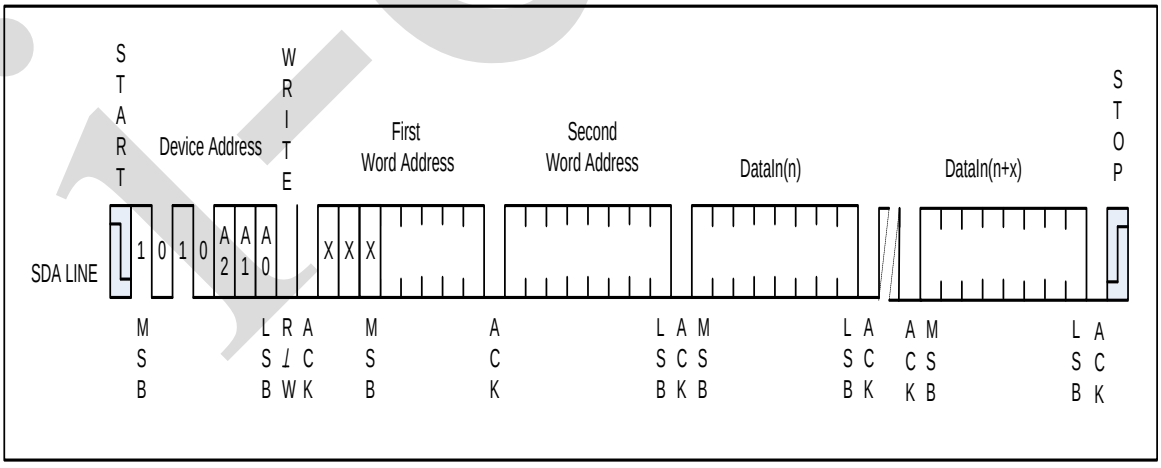


Figure 9

The internal lower six bits of the data word address are automatically incremented after the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at

the beginning of the same page. It means if more than 64 data words are transmitted to the EEPROM, the data word address will roll-over, and previous data will be overwritten.

4.3.3、Acknowledge Polling

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with low level, allowing the read or write sequence to continue.

4.3.4、Write Identification Page

This identification page (64 bytes) is an additional page that can be written and locked in read-only mode permanently. It is coded by writing an identification instruction. The write identification instruction uses the same protocol and format (format, memory) as page writing except for the following differences:

- Equipment type identifier = 1011b;
- When B10 must be "00", it doesn't matter what the highest bits B14 and B6 are.

The lowest bits B5, B0 define the byte address in the identification page. If the identification page is locked, the data byte propagated during the instruction to write the identification page is not acknowledged (i.e. NOACK).

4.3.5、Lock Identification Page

The lock identification page instruction permanently locks the identification page in the read-only mode. This instruction is similar to the write byte instruction, with the following specific conditions:

- Equipment type identifier = 1011b;
- Address bit B10 must be 1, and it doesn't matter how many other address bits are;
- This data byte must be equal to "XXXXXX1X" (X is 0 or 1).

4.4、Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

4.4.1、Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address and the read/write select bit(set to "1") are clocked in and the EEPROM sends response signal, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 10).

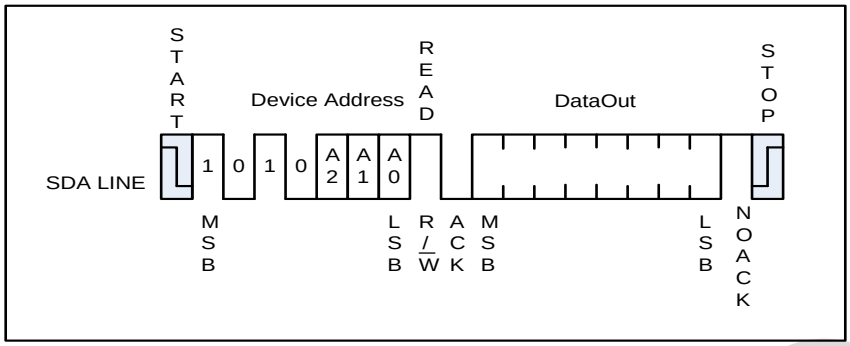


Figure 10

4.4.2、Random Read

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates the address counter by sending a device address(the read/write select bit is "1"). The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a low-level response but generates a following stop condition(see Figure11).

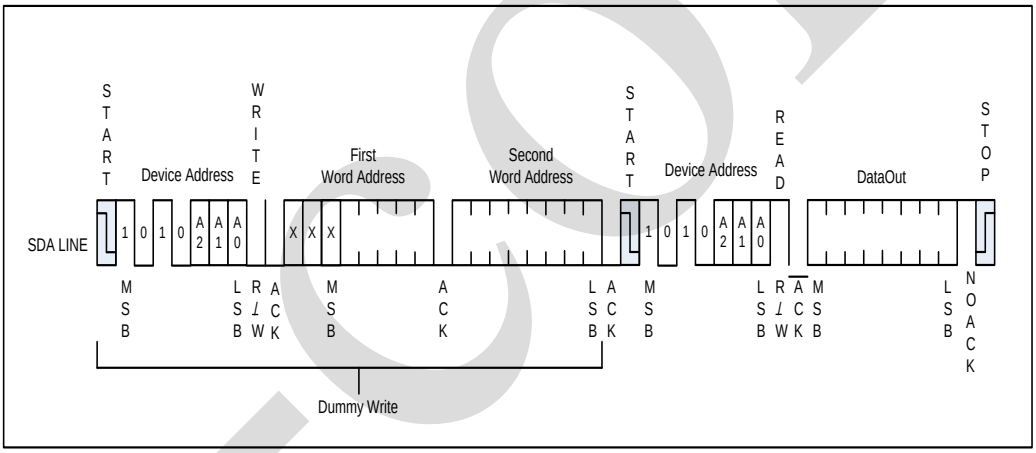


Figure 11

4.4.3、Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the EEPROM receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a low-level response but does generate a following stop condition (see Figure 12)

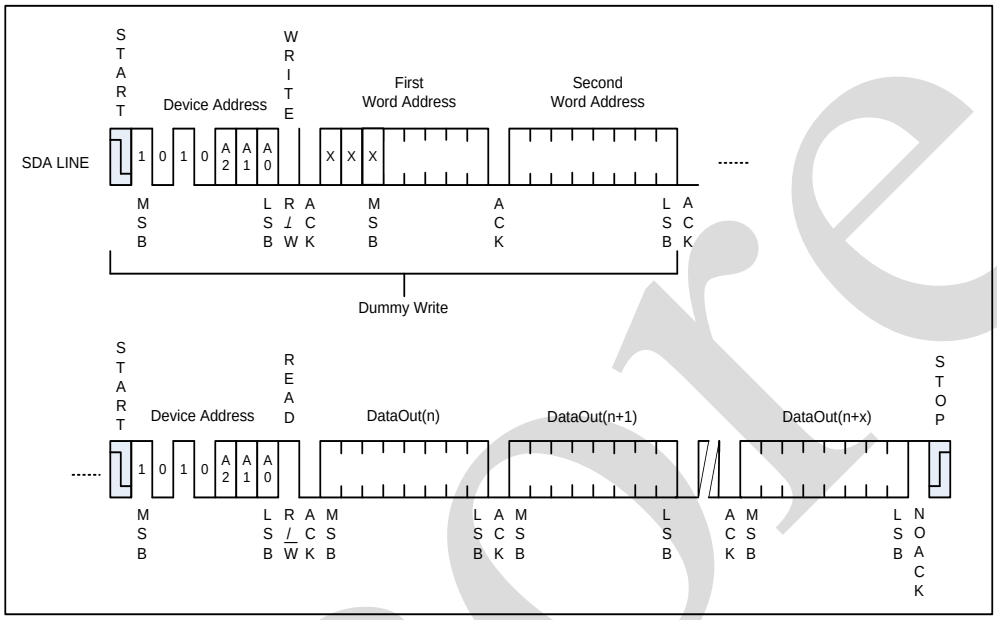


Figure 12

4.4.4、Read Identification Page

This identification page (64 bytes) is an additional page that can be written and locked in read-only mode permanently. The identification page can be coded by reading an identification instruction. The write identification instruction uses the same protocol and format as the read command defined as the device identifier of 1011b. The most significant bits B14 and B6 are irrelevant, while the least significant bits B5 and B0 define the byte address in the identification page. The number of bytes read in the identification page must not exceed the page boundary. (For example, when reading the identification page from 10d, the number of bytes should be less than or equal to 54, because the boundary of the identification page is 64 bytes).

4.4.5、Read Lock State

The locked/unlocked state of the identification page can be checked by sending a specific truncation command to the device. If the identification page is not latched, the device returns an acknowledgement signal. Otherwise, it returns no response. As shown in figure 13.

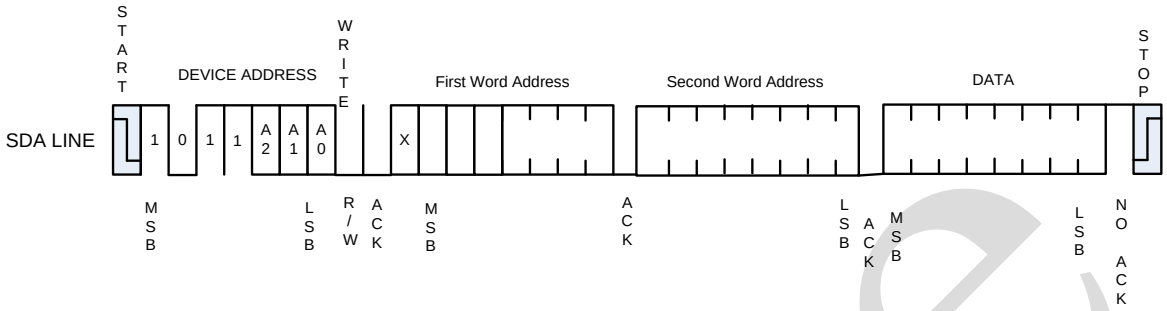
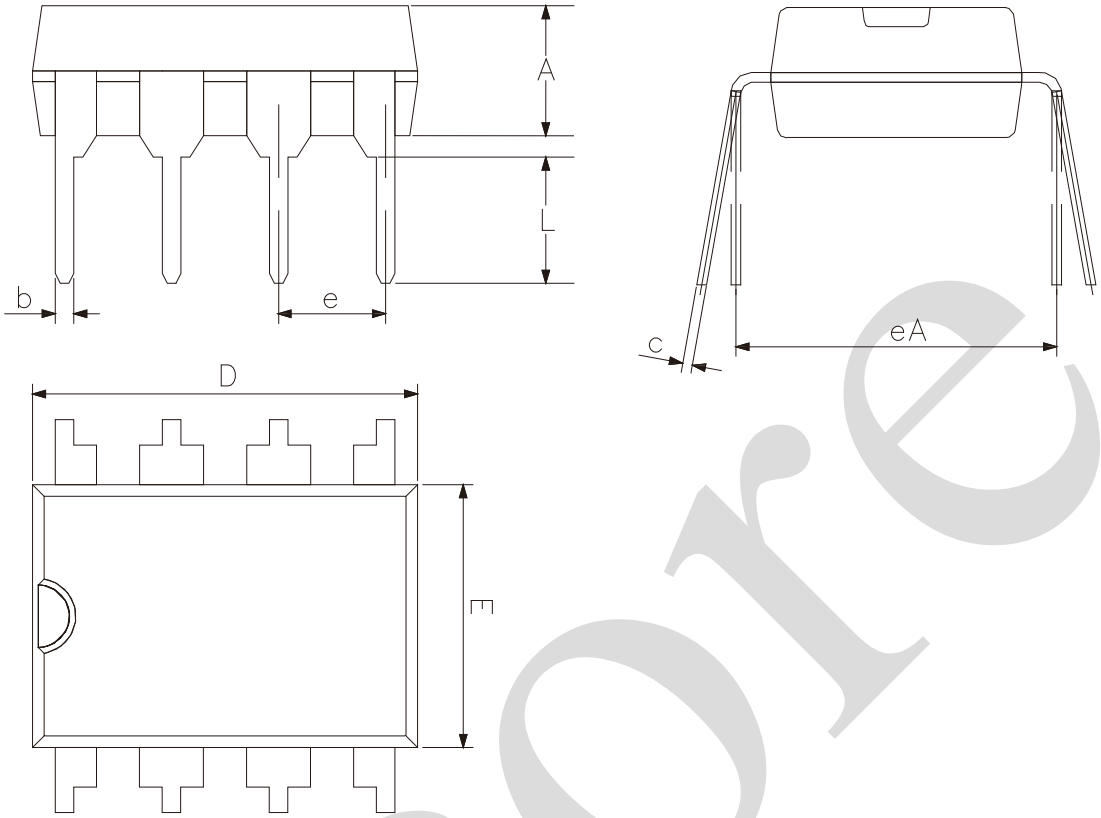


Figure 13

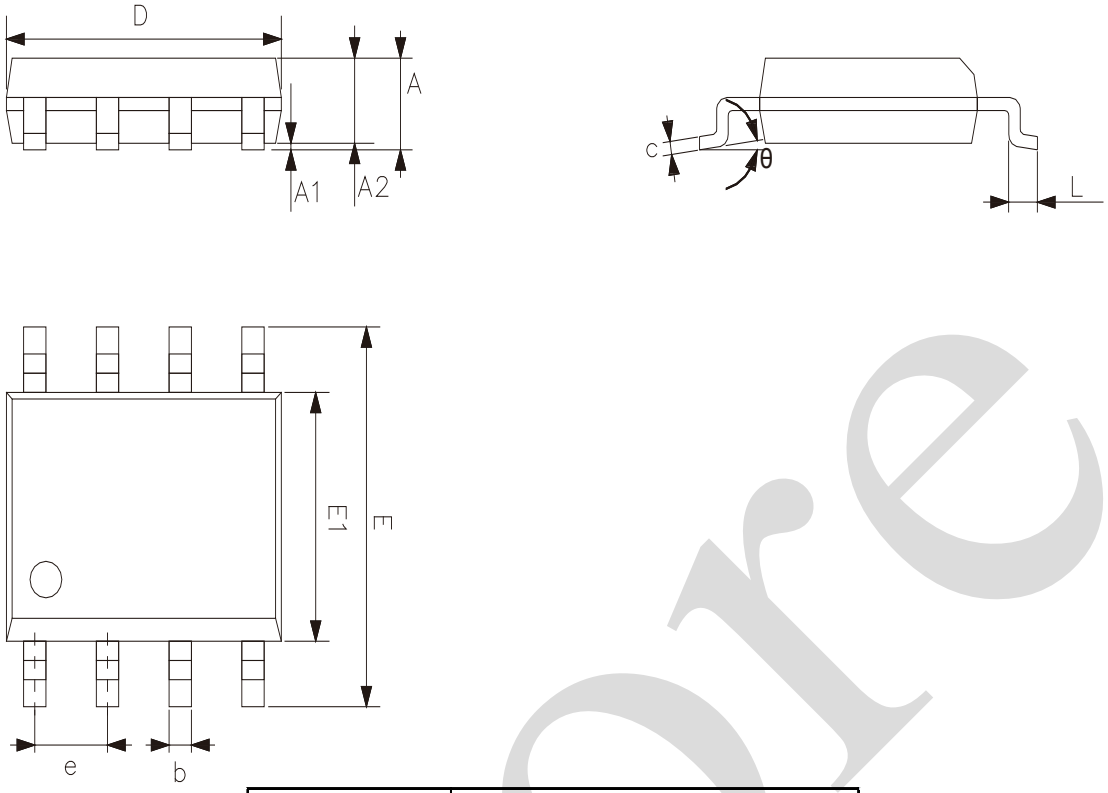
5、P ackage Information

5.1、DIP8



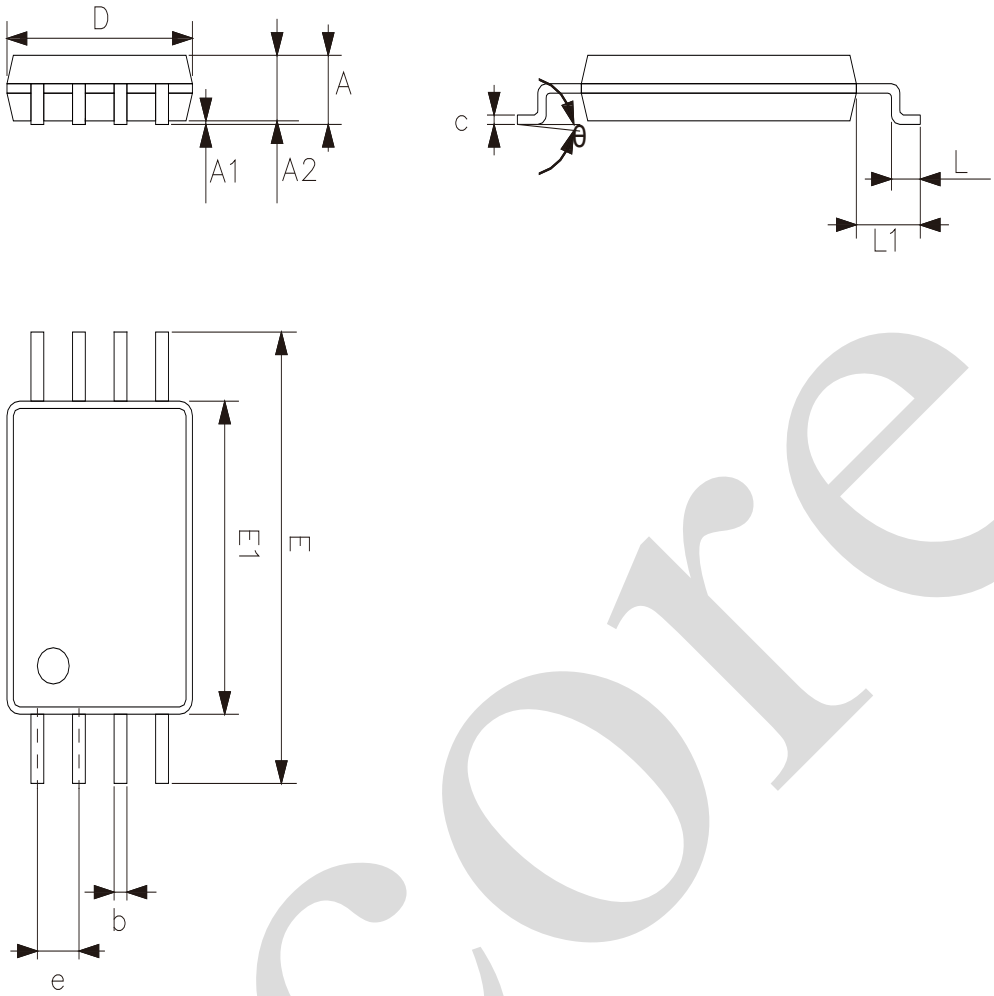
2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	3.00	3.60
b	0.36	0.56
c	0.20	0.36
D	9.00	9.45
E	6.15	6.60
e	2.54	
eA	7.62	9.30
L	3.00	—

5.2、SOP8



2023/12/A	Dimensions In Millimeters	
Symbol	Min.	Max.
A	1.35	1.80
A1	0.05	0.25
A2	1.25	1.55
D	4.70	5.10
E	5.80	6.30
E1	3.70	4.10
b	0.306	0.51
c	0.19	0.25
e	1.27	
L	0.40	0.89
θ	0°	8°

5.3、TSSOP8



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

6、S tatements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We recommend you to read this chapter carefully before using this product.

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