CS4863
Dual 2.2W Class-AB Power Amplifier With Stereo Headphone Function

Product Specification

Specification Revision History:

Version	Data	Description
2010-01-A1	2010-01	New
2012-01-B1	2012-01	Increase the manual number and release history
2024-11-C1	2024-11	Replace the new template; Modify the content

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1、General Description

The CS4863 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.2W to a 4Ω load (Note 1) or 2.5W to a 3Ω load (Note 2) with less than 1.0% THD+N. In addition, the headphone input pin allows the amplifiers to operate in single-ended mode when driving stereo headphones.

Boomer audio power amplifiers were designed specifically to provide high quality output power from a surface mount package while requiring few external components. To simplify audio system design, the CS4863 combines dual bridge speaker amplifiers and stereo headphone amplifiers on one chip. The CS4863 features an externally controlled, low-power consumption shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection. It also utilizes circuitry to reduce “clicks and pops” during device turn-on.

Features:

- Stereo headphone amplifier mode
- “Click and pop” suppression circuitry
- Unity-gain stable
- Thermal shutdown protection circuitry
- DIP16, ETSSOP20 and SOP16 packages

Key Specifications

- PO at 1% THD+N
  CS4863 8Ω 1.1W(typ)
- Single-ended mode THD+N at 75mW into 32Ω 0.5%(max)
- Shutdown current 0.7μA(typ)
- Supply voltage range 2.0V to 5.5V

Ordering Information:

Tube packing specifications:

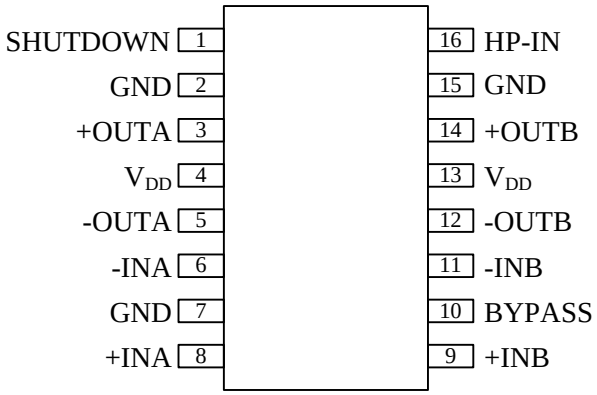
Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CS4863DA16.TB	DIP16	CS4863	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19mm×6.4mm Pin spacing: 2.54mm
CS4863SA16.TB	SOP16	CS4863	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10mm×3.9mm Pin spacing: 1.27mm
CS4863TE20.TB	ETSSOP20	CS4863	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

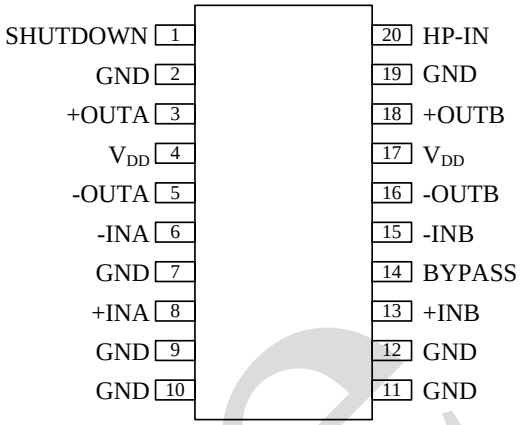
Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CS4863SA16.TR	SOP16	CS4863	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10mm×3.9mm Pin spacing:1.27mm

Note：If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Pin Configurations



SOP16/DIP16



ETSSOP20

3、Electrical Parameter

3.1、Absolute Maximum Ratings

Characteristic	Symbol	Conditions		Value	Unit
Supply Voltage	V_{DD}	-		5.5	V
Input Voltage	V_{IN}	-		-0.3～V_{DD}+0.3	V
Storage Temperature	Tstg	-		-65~+150	℃
Power Dissipation	P_D	-		Internally limited	-
Junction Temperature	Tj	-		150	℃
Temperature Range	Tr	-		-40℃~+85	℃
Soldering temperature	T_L	10s	DIP	245	℃
			SOP/ETSSOP	260	℃
Thermal Resistance	θ_{JC}-M16B	-		20	℃/W
	θ_{JA}- M16B	-		80	
	θ_{JC}- M16A	-		20	
	θ_{JA}- M16A	-		63	
	θ_{JC}-MTC20	-		20	
	θ_{JA}-MTC20	-		80	
	θ_{JC}-MXA20A	-		2	

3.2、Electrical Characteristics

3.2.1、DC Characteristics for Entire IC

(V_{DD}=5V,T_{amb}=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	-	2	-	5.5	V
Quiescent Power Supply Current	I_{DD}	V_{IN}=0V，I_O=0A，HP-IN=0V	6	11.5	20	mA
		V_{IN}=0V，I_O=0A，HP-IN=4V	-	5.8	-	
Shutdown Current	I_{SD}	V_{DD} applied to the SHUTDOWN pin	-	0.7	2	μA
Headphone High Input Voltage	V_{IH}	-	4	-	-	V
Headphone Low Input Voltage	V_{IL}	-	-	-	0.8	V

3.2.2、DC Characteristics for Bridged-Mode Operation

(V_{DD}=5V,T_{amb}=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Offset Voltage	V_{OS}	V_{IN}=0V	-	5	50	mV
Output Power	P_O	THD+N=1%, f=1KHz, R_L=8Ω	-	1.1	-	W
		THD+N=10%, f=1KHz, R_L=8Ω	-	1.5	-	W
		THD+N=1%, f=1KHz, R_L=32Ω	-	0.34	-	W
Total Harmonic Distortion + Noise	THD+N	20Hz≤f≤20KHz, A_{VD}=2, R_L=8Ω, PO=1W	-	0.3	-	%
Power Supply Rejection Ratio	PSRR	V_{DD}=5V, R_L=8Ω, C_B=1.0μF, VRIPPLE=200mV_{RMS}	-	67	-	dB
Channel Separation	X_{TALK}	f=1KHz, C_B=1.0μF	-	-90	-	
Signal To Noise Ratio	SNR	V_{DD}=5V, R_L=8Ω, PO=1.1W	-	98	-	

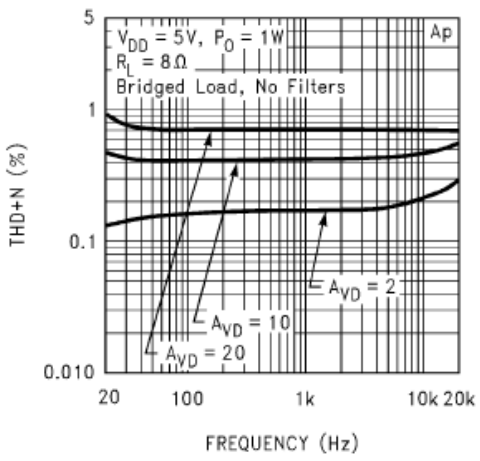
3.2.3 Electrical Characteristics for Single-Ended Operation

(V_{DD}=5V,T_{amb}=25℃)

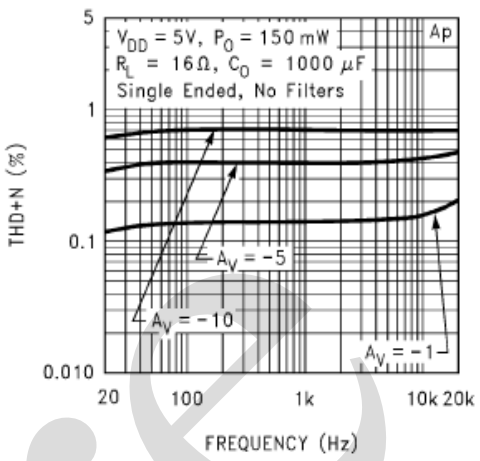
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Offset Voltage	V_{OS}	V_{IN}=0V	-	5	50	mV
Output Power	P_O	THD+N=0.5%, f=1KHz, R_L=32Ω	75	85	-	mW
		THD+N=1%, f=1KHz, R_L=8Ω	-	340	-	
		THD+N=10%, f=1KHz, R_L=8Ω	-	440	-	
Total Harmonic Distortion + Noise	THD+N	20Hz≤f≤20KHz, A_V=-1, R_L=32Ω, P_O= 75mW	-	0.2	-	%
Power Supply Rejection Ratio	PSRR	V_{RIPPLE}=200mV_{RMS}, f=1KHz, C_B=1.0μF	-	52	-	dB
Channel Separation	X_{TALK}	f=1KHz, C_B=1.0μF	-	-60	-	dB
Signal To Noise Ratio	SNR	V_{DD}=5V, R_L=8Ω, P_O=340mW	-	95	-	dB
Power on stabilization time	Tstab	C_B=0.33uF, V_{DD}=5V	-	240	-	ms

4、Characteristic Curve

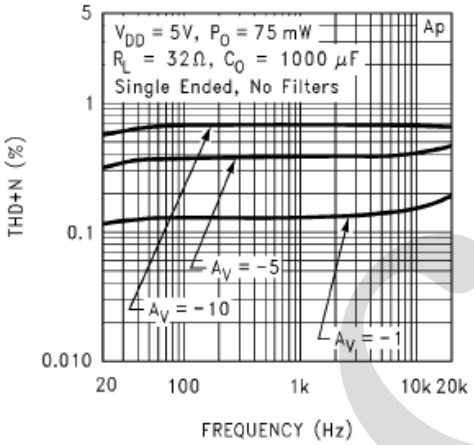
THD+N vs Frequency



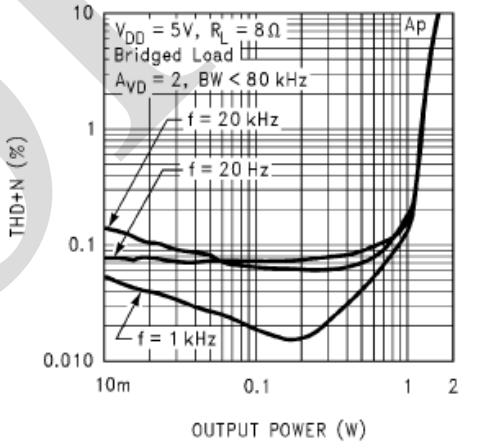
THD+N vs Frequency



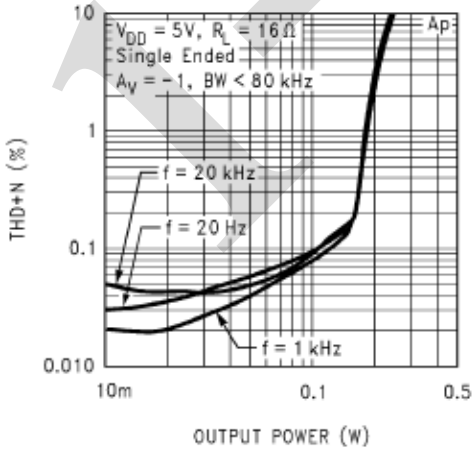
THD+N vs Frequency



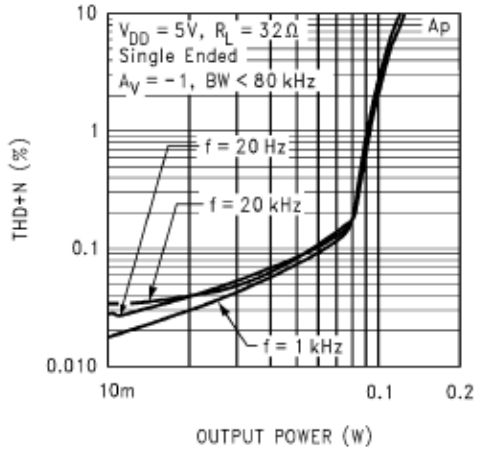
THD+N vs Output Power



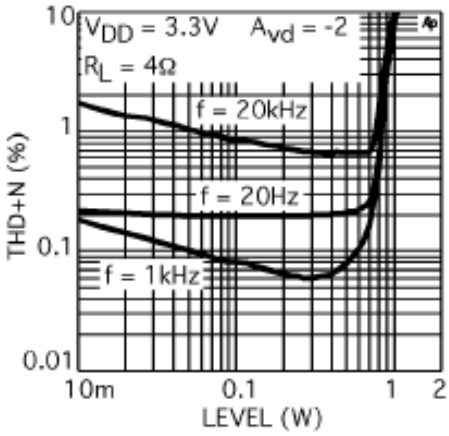
THD+N vs Output Power



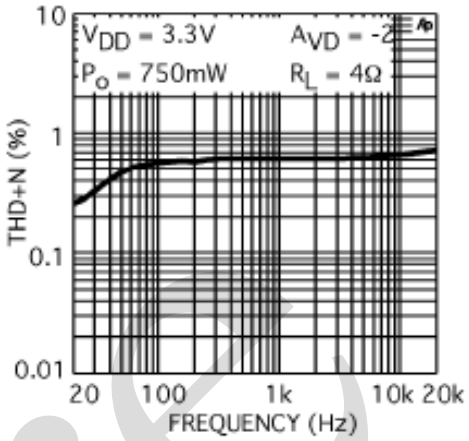
THD+N vs Output Power



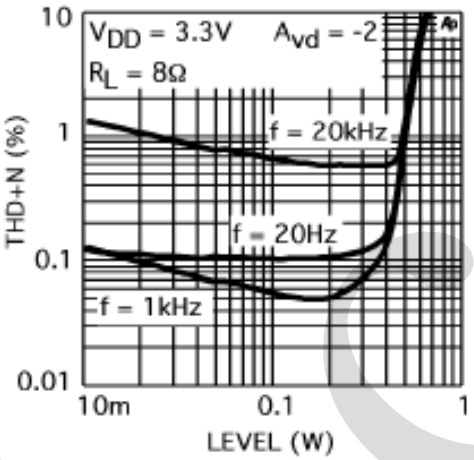
THD+N vs Output Power



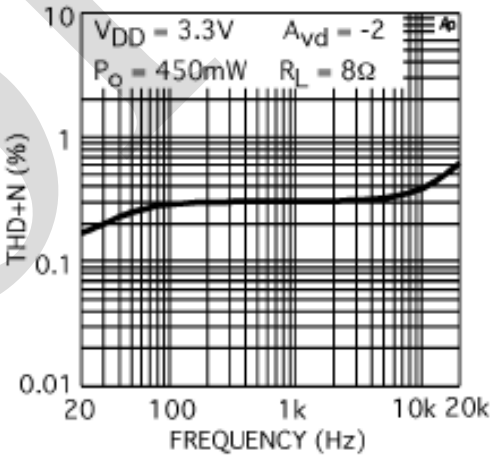
THD+N vs Frequency



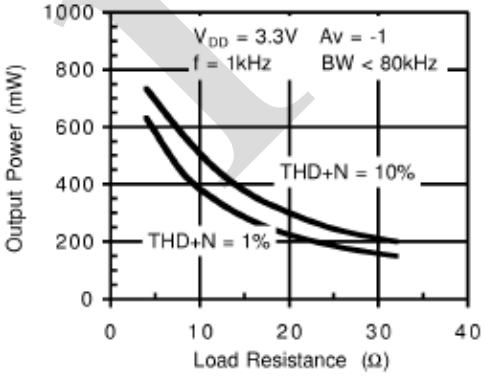
THD+N vs Output Power



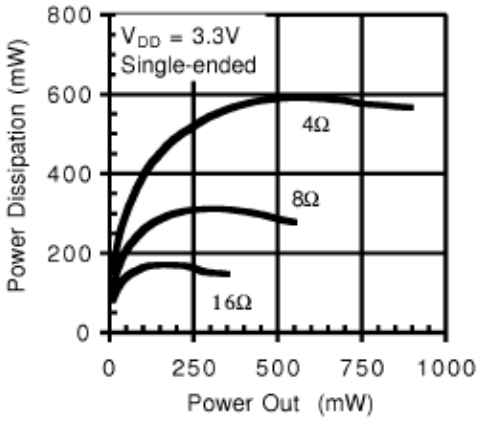
THD+N vs Frequency



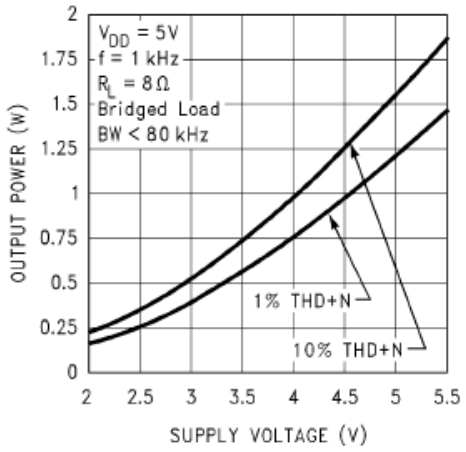
Output Power vs Load Resistance



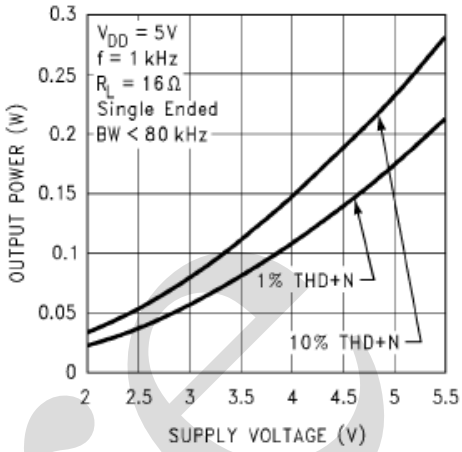
Power Dissipation vs Supply Voltage



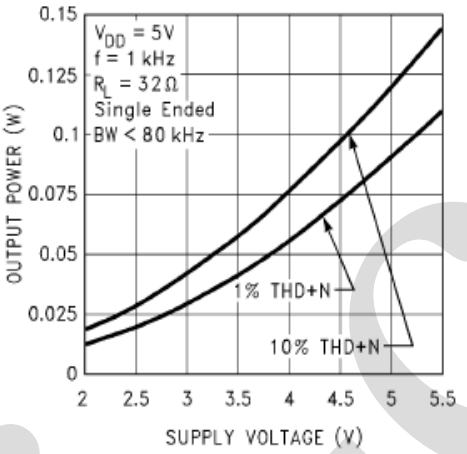
Output Power vs Supply Voltage



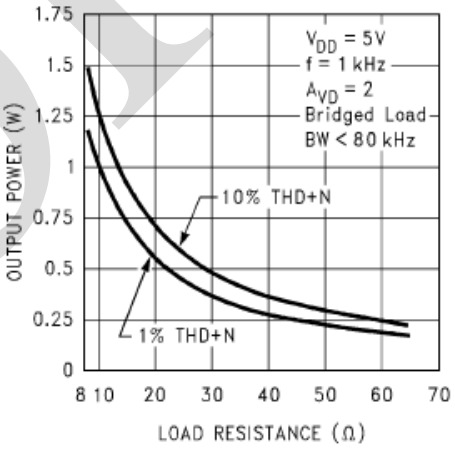
Output Power vs Supply Voltage



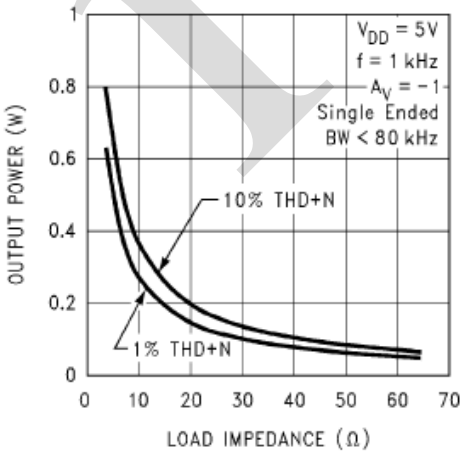
Output Power vs Supply Voltage



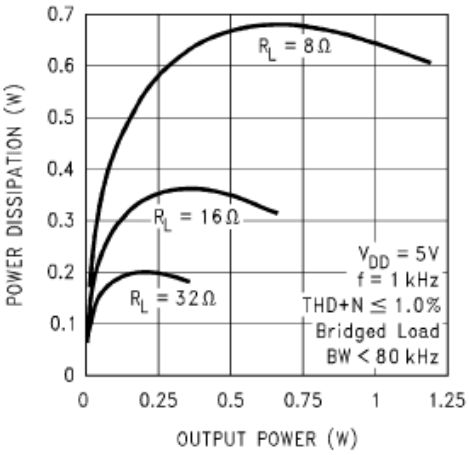
Output Power vs Load Resistance



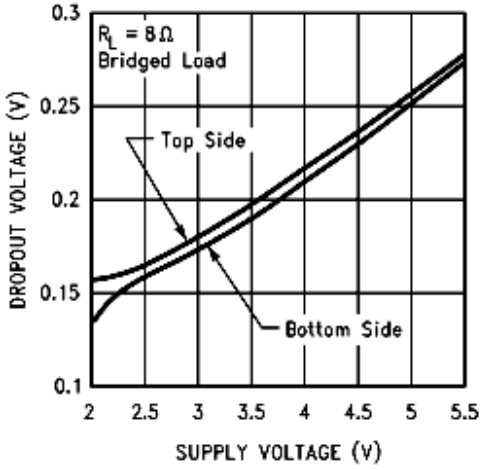
Output Power vs Load Resistance



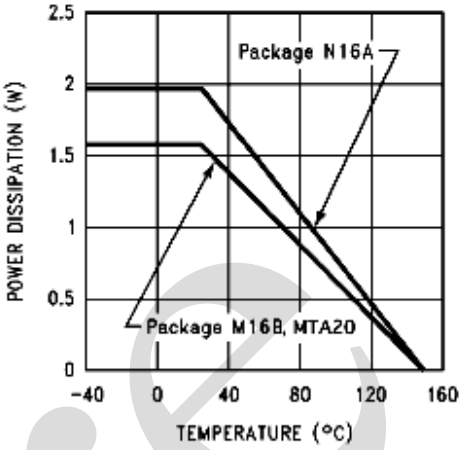
Power Dissipation vs Output Power



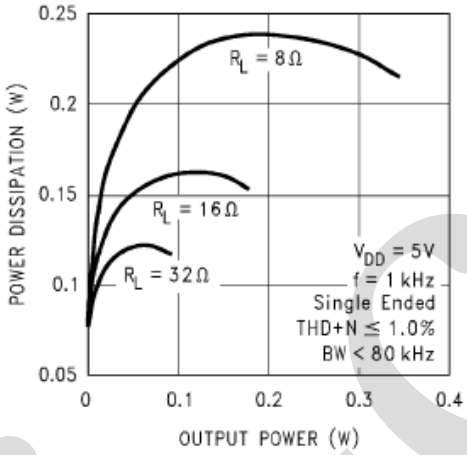
Dropout Voltage vs Supply Voltage



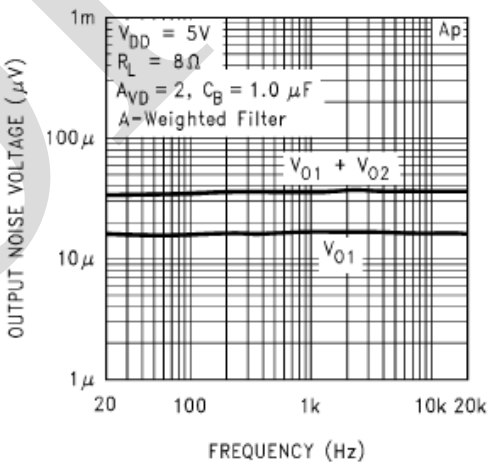
Power Derating Curve



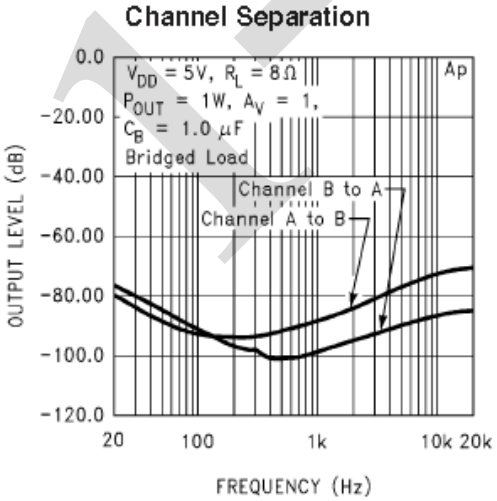
Power Dissipation vs Output Power



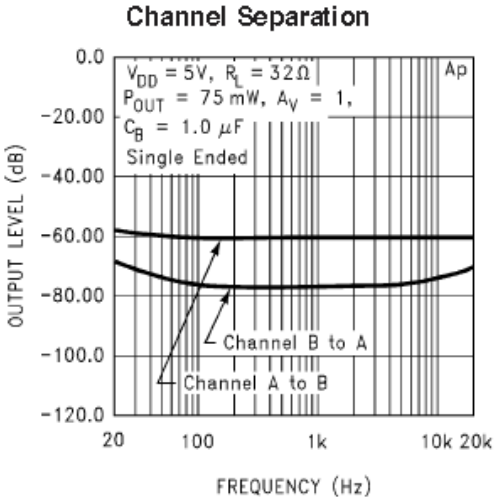
Noise Floor



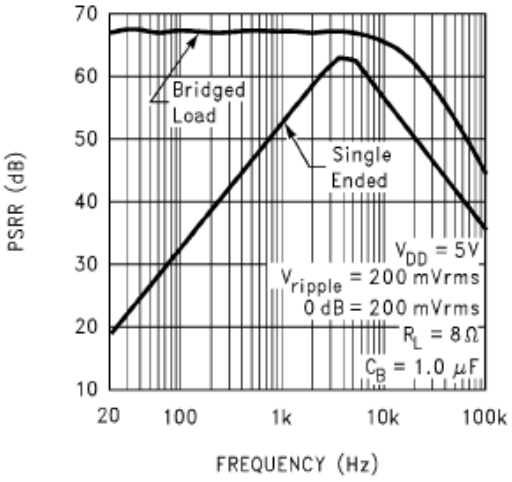
Channel Separation



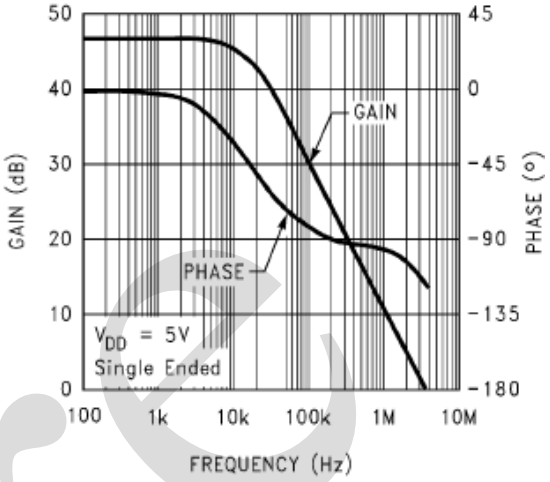
Channel Separation



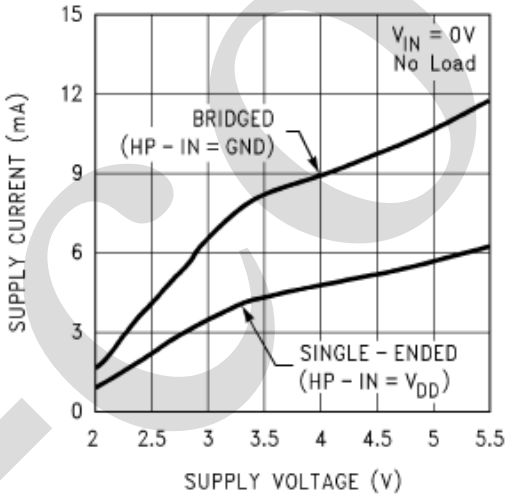
Power Supply Rejection Ratio



Open Loop Frequency Response



Supply Current vs Supply Voltage



5、Typical Application Circuit And Application Note

5.1、Typical Application Circuit

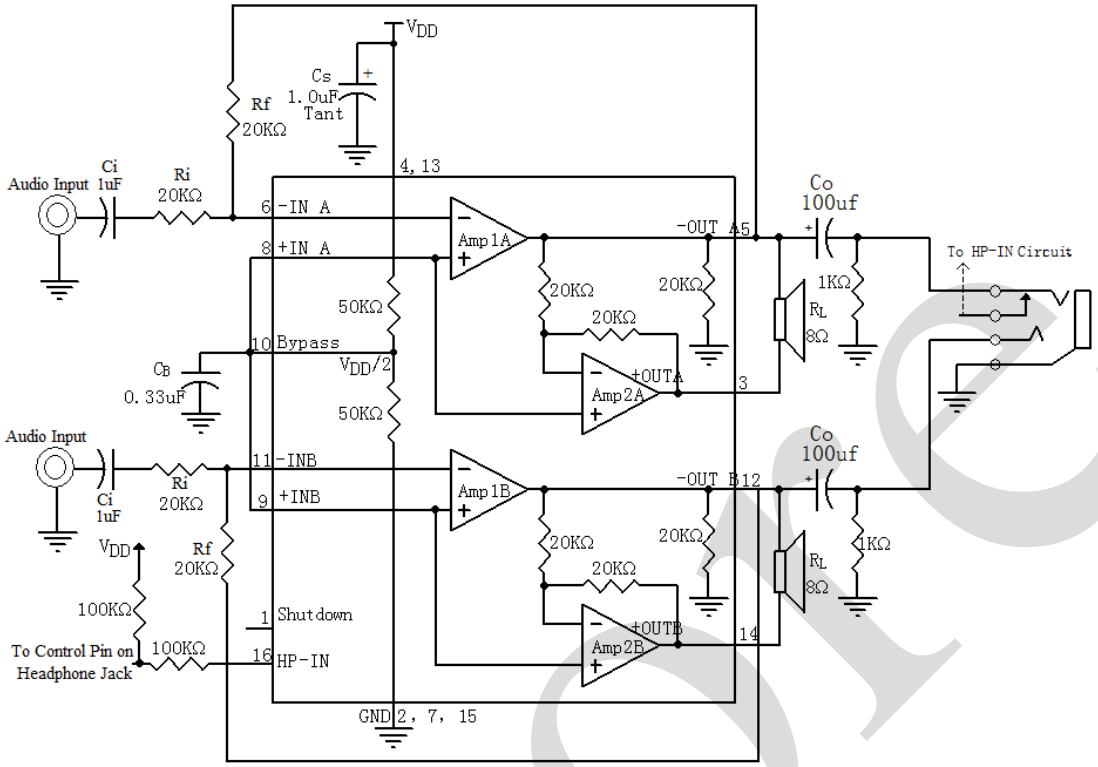


Figure 1

5.2、Application Note

5.2.1、Bridge Configuration Explanation

As shown in Figure 1, the CS4863 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.) External resistors R_f and R_i set the closed-loop gain of Amp1A, whereas two internal 20KΩ resistors set Amp2A's gain at -1. TheCS4863 drives a load, such as a speaker, connected between the two amplifier outputs, -OUTA and +OUTA.

Figure 1 show that Amp1A's output serves as Amp2A's input. This results in both amplifiers producing signals identical in magnitude, but 180°out of phase. Taking advantage of this phase difference, a load is placed between –OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 \times (R_f / R_i) \qquad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

5.2.2、Power Dissipation

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \qquad \text{Single-Ended} \qquad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The CS4863 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (3), assuming a 5V power supply and a 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$$P_{DMAX} = 4 \times (V_{DD})2 / (2\pi^2 R_L) \qquad \text{Bridge Mode} \qquad (3)$$

Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \qquad (4)$$

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the Junction −to− case thermal impedance, CS is the case −to− sink thermal impedance, and θ_{SA} is the sink −to− ambient thermal impedance.) Refer to the "Typical Performance Characteristics "curves for power dissipation information at lower output power levels.

5.2.3、Power Supply Bypassing

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10μF in parallel with a 0.1μF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0μF tantalum bypass capacitance connected between the CS4863's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation in the output signal. Keep the length of leads and traces that connect capacitors between the CS4863's power supply pin and ground as short as possible. Connecting a 1μF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, Proper Selection of External Components), system cost, and size constraints.

5.2.4、Micro-Power Shutdown

The voltage applied to the SHUTDOWN pin controls the CS4863's shutdown function. Activate micro-power shutdown by applying V_{DD} to the SHUTDOWN pin. When active, the CS4863's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically $V_{DD}/2$. The low 0.7μA typical shutdown current is achieved by applying a voltage that is as near as V_{DD} as possible to the SHUTDOWN pin. A voltage that is less than V_{DD} may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 10KΩ pull-up resistor between the SHUTDOWN pin and V_{DD}, or connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to V_{DD} through the pull-up resistor, activating micro-power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

TABLE1. Logic level truth table for SHUTDOWN and HP-IN Operation

SHUTDOWN	HP-IN PIN	OPERATIONAL MODE
Low	logic Low	Bridged amplifiers
Low	logic High	Single-Ended amplifiers
High	logic Low	Micro-power Shutdown
High	logic High	Micro-power Shutdown

5.2.5、HP-IN Function

Applying a voltage between 4V and V_{DD} to the CS4863's HP-IN headphone control pin turns off Amp2A and Amp2B, muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 2 shows the implementation of the CS4863's headphone control function. With no headphones connected to the headphone jack, the R1-R2 voltage divider sets the voltage applied to the HP-IN pin (pin 16) at approximately 50mV. This 50mV enables Amp1B and Amp2B, placing the CS4863's in bridged mode operation. The output coupling capacitor blocks the amplifier's half-supply DC voltage, protecting the headphones.

While the CS4863 operates in bridged mode, the DC potential across the load is essentially 0V. The HP-IN threshold is set at 4V. Therefore, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from -OUTA and allows R1 to pull the HP Sense pin up to V_{DD}. This enables the headphone function, turns off Amp2A and Amp2B, and mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistor R2 and R3. These resistors have negligible effect on the CS4863's output drive capability since the typical impedance of headphones is 32Ω.

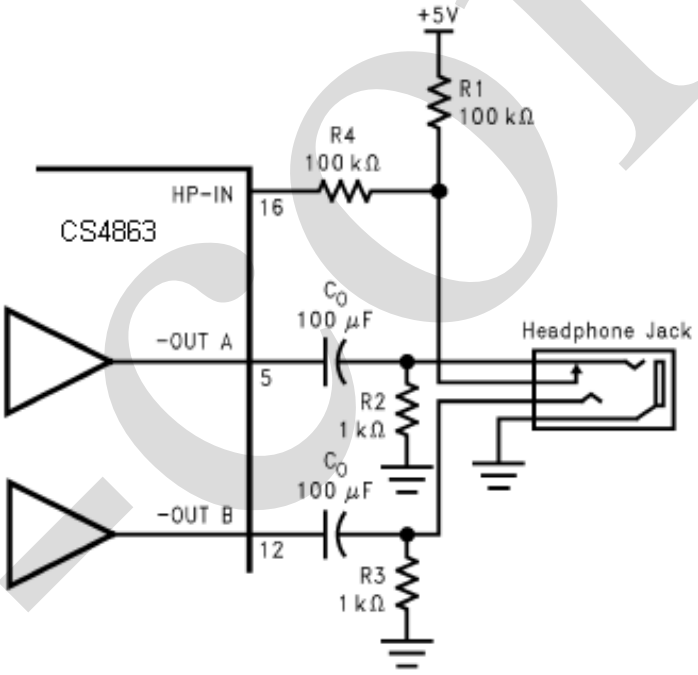


Figure2. Headphone Circuit

Figure 2 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP-IN pin when connecting headphones.

A microprocessor or a switch can replace the headphone jack contact pin. When a microprocessor or switch applies a voltage greater than 4V to the HP-IN pin, a bridge-connected speaker is muted and Amp1A and Amp2A drive a pair of headphones.

5.2.6、Selecting Proper External Components

Optimizing the CS4863's performance requires properly selecting external components. Though the CS4863 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The CS4863 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$).

5.2.7、Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, C_I has an effect on the CS4863's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_f. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency.

A shown in *Figure 1*, the input resistor (RI) and the input capacitor, C_I produce a -3dB high pass filter cutoff frequency that is found using Equation (5).

$$f_{-3dB} = \frac{1}{2\pi R_i C_i} \qquad (5)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_I, using Equation (5), is 0.063μF. The 1.0μF C_I shown in Figure 1 allows the CS4863 to drive high efficiency, full range speaker whose response extends below 30Hz.

5.2.8、Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the CS4863 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the CS4863's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0μF along with a small value of C_i (in the range of 0.1μF to 0.39μF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops.

5.2.9、Optimizing Click And Pop Reduction Performance

The CS4863 contains circuitry to minimize turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the CS4863's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a Controlled linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. Although the bypass pin current cannot be modified, changing the size of C_B alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of C_B and the turn-on time. Here are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.01μF	20 ms
0.1μF	200 ms
0.22μF	440 ms
0.47μF	940 ms
1.0μF	2 Sec

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops". In a single-ended configuration, the output is coupled to the load by C_{OUT}. This capacitor usually has a high value. C_{OUT} discharges through internal 20KΩ resistors. Depending on the size of C_{OUT}, the discharge time constant can be relatively large. To reduce transients in single-ended mode, an external 1KΩ~5KΩ resistor can be placed in parallel with the internal 20KΩ resistor. The trade off for using this resistor is increased quiescent current.

5.2.10、No Load Stability

The CS4863 may exhibit low level oscillation when the load resistance is greater than 10KΩ. This oscillation only occurs as the output signal swings near the supply voltages. Prevent this oscillation by connecting a 5KΩ between the output pins and ground.

5.2.11、Audio Power Amplifier Design(Audio Amplifier Design: Driving 1W into an 8Ω Load)

The following are the desired operational parameters:

Power Output:	1Wrms
Load Impedance:	8Ω
Input Level:	1Vrms
Input Impedance:	20KΩ
Bandwidth:	100Hz−20 kHz ±0.25 dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs. Supply Voltage curve in the "Typical Performance Characteristics" section. Another way, using Equation (6), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs. Supply

Voltage in the "Typical Performance Characteristics "curves, must be added to the result obtained by Equation (6). The result is in Equation (7).

$$V_{OPEAk}=(2R_LP_O) \quad (6)$$

$$V_{DD}\geqslant(V_{OUTPEAk}+(V_{ODTOP}+V_{ODBOG})) \quad (7)$$

The Output Power vs. Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. The commonly used 5V supply voltage easily meets this. The additional voltage creates the benefit of headroom, allowing the CS4863 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the "Power Dissipation" section.

After satisfying the CS4863's power dissipation requirements, the minimum differential gain is found using Equation (8).

$$A_{VD} \geq \sqrt{P_O R_L}\,/(V_{IN}) = V_{orms}/V_{inrms} \quad (8)$$

Thus, a minimum gain of 2.83 allows the CS4863's to reach full output swing and maintain low noise and THD+N performance. For this example, let A_{VD} = 3.

The amplifier's overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (9).

$$R_f/R_i = A_{VD}/2 \quad (9)$$

The value of R_f is 30KΩ.The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one −fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \quad (10)$$

and an

$$F_H = 20kHzx5 = 100kHz \quad (11)$$

As mentioned in the "External Components" section, R_i and C_i create a high-pass filter that sets the amplifier's lower band-pass frequency limit. Find the coupling capacitor's value using Equation (12).

$$Cj \geq \frac{1}{2\pi R_i f_C} \quad (12)$$

the result is

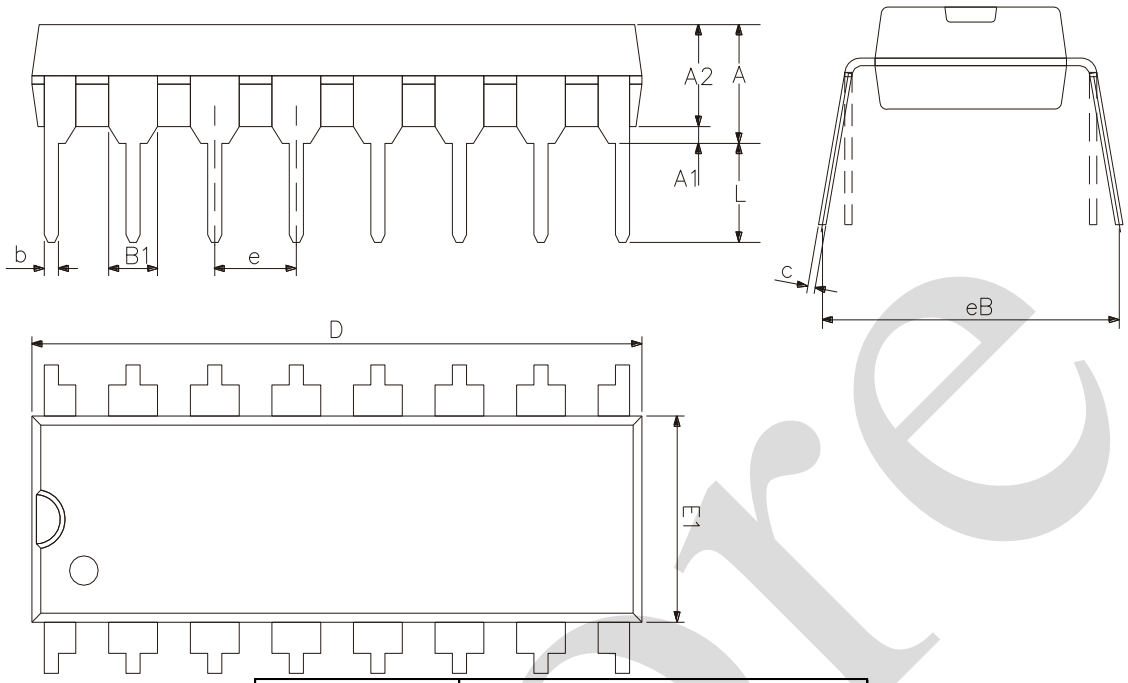
$$1/(2\pi*20K\Omega*20Hz) = 0.398\mu F \quad (13)$$

Use a 0.39μF capacitor, the closest standard value.

The product of the desired high frequency cut off (100 KHz in this example) and the differential gain, A_{VD}, determines the upper pass-band response limit. With A_{VD}= 3 and f_H =100 KHz, the closed-loop gain bandwidth product (GBWP) is 300 KHz. This is less than the CS4863's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-restricting bandwidth limitations.

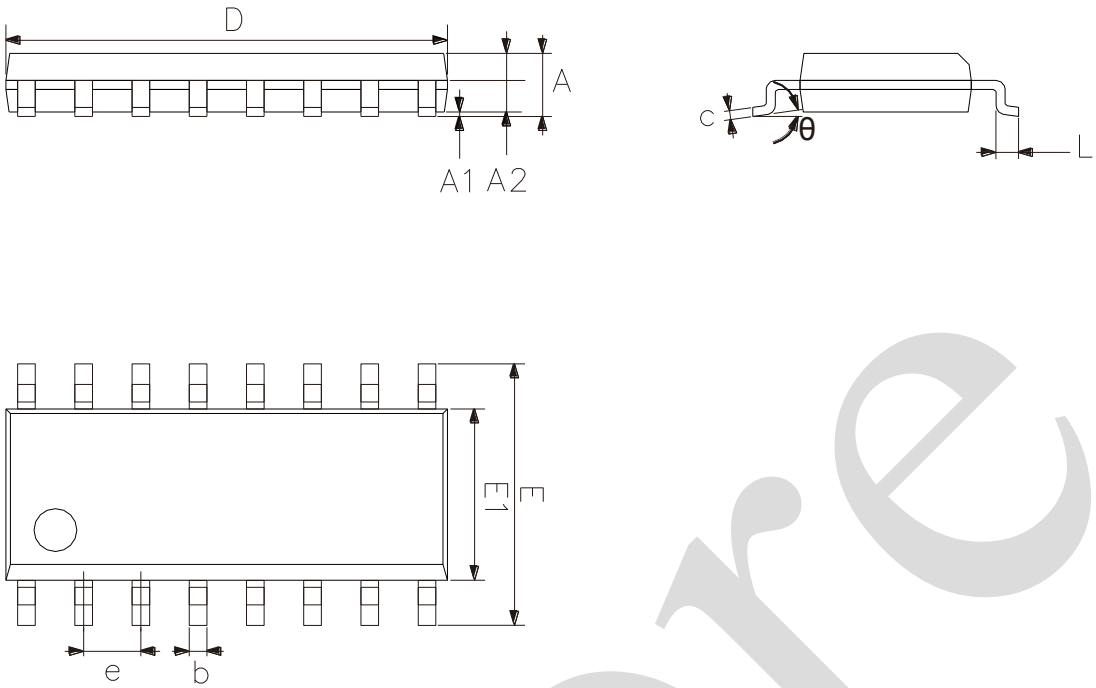
6、Package Information

6.1、DIP16



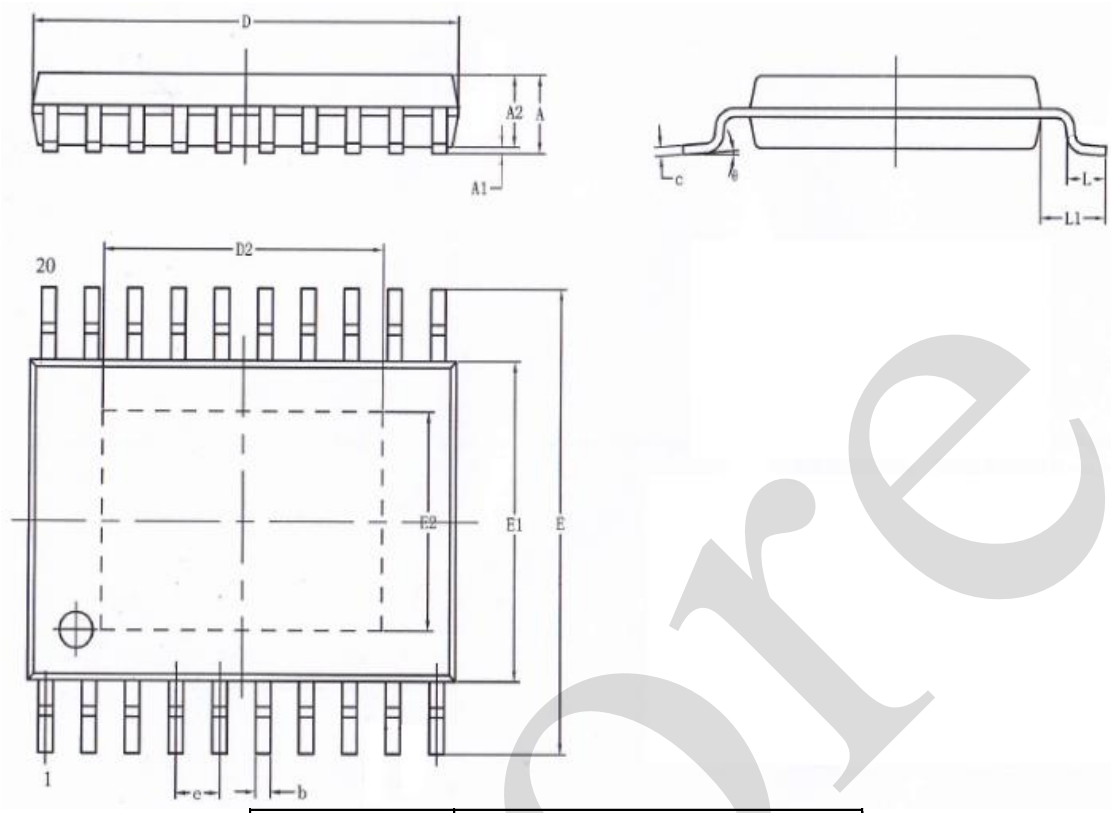
2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A2	3.00	3.60
A1	0.51	—
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

6.2、SOP16



2023/12/A	Dimensions In Millimeters	
Symbol	**Min.**	**Max.**
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

6.3、ETSSOP20



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	—	1.20
A1	0.02	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
D2	4.10	4.30
E	6.20	6.60
E1	4.30	4.50
E2	2.90	3.10
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

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